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SWITZERLAND

Patents ADP number *(if you know it)* 7473739001

If the applicant is a corporate body, give the country/state of its incorporation International Organisation

4. Title of the invention

A Sensing and Imaging Device

5. Name of your agent *(if you have one)*

Anna E Reeve

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

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A Sensing And Imaging Device

The invention relates to a sensing device and imaging devices comprising a plurality of the sensing devices. In particular, the invention relates to a pixel cell and an array of pixel cells arranged to form an imaging device.

BACKGROUND OF THE INVENTION

Conventional pixel radiation sensors are often based on a hybrid approach in which an electronic circuit is bump bonded to a pixel sensor.

There are a number of types of conventional semiconductor imagers and sensors based on the one hand on a hybrid arrangement for two-dimensional single particle detection, or single photon detection, and on the other hand on active pixel sensors (APS) that are monolithic solid state imagers that include, for each pixel, radiation-sensing, charge-to-voltage conversion, and a reset function.

The hybrid pixel sensor arrangement is mainly used for IR focal planes, Silicon Pixel arrays for single particle detection, X-ray detection and medical imaging. The hybrid pixel sensor permits independent optimisation of the radiation detector characteristics and the pixel readout electronics because they are fabricated on two separate substrates with two different processes. However, this type of pixel sensor has a limit to the minimum achievable pixel dimensions due to the bump bonding technique. So far 50μm x 50μm has been achieved, but it is expensive and complex to fabricate. Moreover, the hybrid pixel sensor has a relatively large input capacitance (100fF to 200fF) which limits its ultimate noise performance.

Monolithic APS's are mainly used for visible light imaging together with CCD imagers, but have also been applied for single particle detection.

All known monolithic APS devices employ a floating diffusion as a pixel sensor in the form of an n-diffusion/n-well in p-doped silicon substrate, a photo-gate, or a PIN diode formed in amorphous Si:H deposited above the integrated circuit. All those sensor types have the pixel signal current integrated on the input capacitance during an integrating time period of few a milliseconds before being read out by a source follower MOSFET transistor F1 as shown in Figure 1 (prior art). Pixel select transistor F3 switches the output of the pixel to a common load F4. The floating node which comprises the junction of the gate of the source follower MOSFET transistor F1, the pixel sensor and the drain of F2, is sequentially reset by means of reset MOSFET transistors F2 as shown in Figure 1. This has the disadvantage of generating a KTC reset noise far above the intrinsic electronic noise of the amplifier stage. Furthermore, the device shown in Figure 1 is not capable of discriminating between incident quanta (hits) during the integration period and therefore is not capable of single particle detection.

For single charged particle detection, the conventional monolithic APS uses, as the sensor element, an 8-12 ohm few microns thick epitaxial layer of the silicon wafer used in standard commercial CMOS technologies. The charge signal collected is, for example, of the order of 80 e- for a minimum ionising charged particle traversing a 1μm thick silicon layer. The major drawback of the conventional bulk silicon sensor is that charge collection is achieved by thermal diffusion of carriers. This intrinsically limits carrier velocity and

thus charge collection is slow, and is spread over adjacent pixels and not complete.

For single photon detection using an integrated APS with an avalanche gain of, for example, 50, the collected charge per photon may be 50 e-. For such very low signal levels, conventional APS architecture is marginally usable, if at all, as the signal-to-noise ratio required to detect one visible photon, one X-ray or one charged particle should be at least 10 to minimise background noise. This requires a noise floor below 5 e- rms, which cannot be achieved by the conventional APS integrating architectures, which have a conversion gain in the order of 20 μV/e- and a reset noise level of greater than 10 e- rms.

Moreover, the integrating APS architecture of conventional devices cannot measure the timing of particle events, and cannot digitally count each incoming charged particle or X-ray or visible photon. Conventional circuit architectures for hybrid pixel radiation sensors are generally too large, typically, at best 50μm x 50μm, and consume too much power, for example 30 to 50 μW, and are consequently not usable for monolithic integration of high density pixel sensors with quantum detection capability. Therefore, no known electronic circuit exists that can process the very low signals required for Single Particle/Photon Detection and imaging (SPD) in monolithic integrated circuits.

The present invention aims to substantially overcome or ameliorate one or more of the aforementioned problems. In particular, the present invention, in one or more embodiments attempts to solve the problems of monolithic integration of active silicon pixels in commercial deep submicron CMOS

technologies and aims to achieve single particle detection, spatial localisation of single charged particle tracks and single photon detection in contrast to conventional APS designs which integrate the sensor signal current over a certain integrating time period.

SUMMARY OF THE DISCLOSURE

According to the present invention in a first aspect there is provided a sensing device comprising a sensor for detecting arrival of an incident quantum of electromagnetic radiation and/or charged particles, and an amplifier connected to the sensor for amplifying a signal from the sensor, wherein the sensor and the amplifier are fabricated on a common substrate, the sensing device being arranged to discriminate between the arrival of single or multiple incident quanta at the sensing device.

Preferably, the sensor and the amplifier are diffused onto the common substrate, or are deposited on the common substrate. Preferably, the sensing device is a pixel cell.

In a preferred embodiment, the substrate comprises a monolithic semiconductor integrated circuit substrate and the sensor comprises a p-n junction sensor overlaying the substrate, a p-n photodiode, an avalanche photodiode integrated in the substrate, or a radiation sensor for detecting charged particles and/or X-ray photons.

In a preferred embodiment, the substrate comprises a silicon crystal bulk into which the sensor and amplifier are introduced.

Preferably, the sensing device further comprises an amorphous Si:H PIN diode having a plurality of amorphous Si:H layers comprising an Ndoped layer, an Intrinsic layer, and a Pdoped layer, the layers being deposited above the substrate. In an alternative embodiment, the sensing device further comprises an amorphous selenium layer, the amorphous selenium layer being deposited above the substrate. The use of an amorphous selenium layer is particularly advantageous in X-ray applications, such as mammogram procedures. It has a higher conversion efficiency for X-ray photons of energy above 10 KeV than that provided when amorphous Si:H is used.

Preferably, the amplifier comprises a non-linear transresistance amplifier.

In further preferred embodiments, the sensor and the amplifier may be diffused onto the substrate or deposited onto the substrate.

According to the present invention in a second aspect there is provided a device for producing a signal corresponding to a detection event comprising one or more of the sensing devices defined above, further comprising a readout circuit for receiving the output of one or more of the sensing devices and producing an output signal corresponding to the detection event.

Preferably, the device further comprises a detection plane array of the sensing devices defined above.

In a preferred embodiment, the readout circuit is a complementary metal oxide semiconductor (CMOS) circuit formed on the substrate and,

preferably, the substrate is of a first conductivity type, the CMOS circuit comprising one or more metal oxide field effect transistors of a first conductivity type, a well region of a second conductivity type in said substrate, and one or more metal oxide semiconductor transistors of a second conductivity type formed in the well region.

Preferably, the readout circuit comprises a first section and a second section. Also, preferably the first section comprises a non-linear transresistance amplifier.

In a preferred embodiment, the non-linear transresistance amplifier comprises a transconductance amplifier, a feedback field effect transistor, and an input current source.

Preferably, the second section comprises a transistor discriminator for generating a binary signal for each quantum of electromagnetic energy and/or charged particle detected.

Preferably, the device is arranged to detect each quantum impinging upon each sensing device in Single Particle Detection (SPD) mode.

Preferably, the device is arranged to integrate charges and sequentially reading the charges out in standard APS operation mode.

In a preferred embodiment, the sensor is a p-n sensor or p-i-n sensor, and the amplifier has an input sensing node, the input sensing node being connected

to the drain of the feedback field effect transistor, the electrode of the sensor and the drain of the input current source.

Preferably, the readout circuit has an output current, and the readout circuit is arranged to receive external reference signals, the external reference signals comprising a Voltage Reference, a Current Reference, and a Bias Current, wherein the external reference signals and the output current from the readout circuit are common to the one or more sensing devices.

Preferably, the feedback field effect transistor has its source connected to the output of the transconductance amplifier.

In a preferred embodiment, the feedback field effect transistor is arranged such that the feedback field effect transistor has a drain current equal to a reference current mirrored by the input current source when the feedback field effect transistor is biased in weak inversion, the field effect transistor forming the input current source, and the feedback field effect transistor DC biasing the sensor.

Preferably, the feedback field effect transistor is arranged such that when biased at a low current between around 1-20pA the current decreases when an input signal occurs at the input sensing node by a particle or photon impinging on the p-n or p-i-n sensor.

Preferably, the transconductance amplifier is in closed-loop when said feedback field effect transistor operates as a feedback network and has a drain current above zero.

In a preferred embodiment, the transconductance amplifier is arranged to operate like a transresistance stage with the feedback field effect transistor operating as a feedback network.

Preferably, the feedback field effect transistor is arranged such that when the feedback field effect transistor turns off for an input signal charge above a threshold value the feedback field effect transistor has a drain current of about zero.

Preferably, the quantum provides an input charge to the sensor, wherein the input threshold charge is around 10 to 15 e- at a reference current of around 10pA.

Preferably, the non-linear transresistance amplifier is arranged to be in open loop when the feedback field effect transistor turns off for an input signal above threshold.

Preferably, the non-linear transresistance amplifier has a low gain for small input signals below threshold when the feedback transistor is turned on, and the non-linear transresistance amplifier has a large gain for signals above threshold when the feedback transistor is turned off.

In a preferred embodiment, the discriminator transistor has its gate connected to the output of the amplifier, and its drain connected to the output of the sensing device, the output port of the sensing device being connected to the output signal, the output signal being a current.

Preferably, the readout circuit is arranged to receive a Voltage Reference, the Voltage Reference establishing the voltage of the output node of the transconductance amplifier through gate-to-source voltage of the feedback transistor.

Preferably, the voltage reference is arranged to bias the transistor discriminator in weak inversion at a drain current of few nanoamps.

Preferably, the quantum impinges on one or more of the sensing devices generating a voltage across the sensor forming an input sensing node voltage, the input sensing node voltage decreasing and output voltage of the transconductance amplifier increasing when the quantum impinges on one or more of the sensing devices.

Preferably, the device is arranged such that when a voltage increases of the output node of the transconductance amplifier occurs, the drain current of the discriminator transistor increases as the exponential of the voltage variation of the output voltage of the transconductance amplifier.

Preferably, the drain current increase of the discriminator transistor is 1000 times (3 current decades) its value between around 1nA to 1μA for an output voltage increase of the transconductance amplifier of about 250 mV.

In a preferred embodiment, the current drain increase of the transistor discriminator switches the voltage of the output port of the sensing device and generates a binary signal.

Preferably, an output voltage increase of about 250 mV is generated by an input charge of about 25 e^-.

Preferably, the readout circuit is arranged to receive a Voltage Reference giving a Voltage Reference value, the Voltage Reference value determining the standby current of the discriminator transistor to provide a discrimination threshold of the readout circuit.

Preferably, the readout circuit comprises an integrating active pixel sensor (APS) imager.

Preferably, the integrating imager includes a source follower stage in place of a discriminator transistor.

Preferably, the integrating imager has an input current source, the input current source being switched off during integrating time and readout time.

In a preferred embodiment, the input current source is periodically biased at about 10pA during the reset time.

Preferably, the device is arranged such that the feedback transistor switches off when the input signal rises above threshold to open the loop around the amplifier to cause a large increase in gain of the amplifier and thereby heighten the sensitivity of the one or more sensing devices.

Preferably, the amplifier comprises a non-linear amplifier having an output and an input, the amplifier being arranged to have a feedback capacitance minimised to around 10^{-17} F for obtaining a charge-to-voltage conversion gain of about 5mV to 10mV at its output for each electron entering its input.

Preferably, the device is an imaging device for producing an output signal corresponding to a detected image.

According to the present invention in a third aspect, there is provided a macro-pixel comprising an array of sensing devices defined above, wherein the outputs of the sensing devices are commoned to give the effect of a larger pixel. The outputs of the pixels may be connected to a bus. Preferably, the macropixel is configured such that if a sensing device in the macropixel should fail, the macropixel will continue to be operable but at a reduced sensitivity.

According to the present invention in a fourth aspect there is provided an array of macropixels defined above connected to detect or form an image.

According to a fifth aspect of the invention there is provided a device comprising an array of the macropixels defined above wherein the imaging device is diffused into or deposited onto the surface of a wafer.

The invention, in one or more embodiments, is applicable to semiconductor imaging and radiation detection devices, in particular to monolithic silicon active pixel sensor arrays capable of detecting single photons or particles, such as visible light, X-rays, and charged particles such as electrons or

protons. The monolithic approach allows fabrication in a standard CMOS process.

In a preferred embodiment, the invention is embodied in an imaging device formed as a monolithic, complementary metal oxide semiconductor integrated circuit in an industrial standard metal oxide process. The pixel integrated circuit preferably includes an amorphous Si:H PIN diode for collecting single photon/particle-generated charge deposited above the integrated circuit overlying the substrate, or an n-well junction or other diode in an underlying region of the epitaxial layer and bulk substrate. The pixel integrated circuit also preferably includes, a readout circuit having at least a transconductance amplifier, and an N-MOSFET feedback device in the p-doped substrate. The N-MOSFET feedback device is preferably connected between the sensing node formed by the connection of the input of the transconductance amplifier with the pixel sensor electrode and the output node of the transconductance amplifier.

In a preferred embodiment, the transconductance amplifier is a four-device circuit formed by two P-MOSFET transistors and two N-MOSFET transistors. In this embodiment, the two P-MOSFET transistors operate as a high gain input cascode amplifier circuit with the input gate connected to the sensor element which could preferably be an N-well electrode, or the PIN amorphous Si:H diode. The two N-MOSFET transistors operate as a high impedance cascode output current source. This preferred embodiment includes an N-MOSFET feedback device that is biased in deep weak inversion by an additional input current source P-MOSFET, which forms,

together with a diode connected P-MOSFET, a current mirror that is biased by an external current source.

Preferably, the feedback MOSFET transistor is biased to a sufficiently low current, for example between 1pA to 20pA, to enable it to be switched off when a small input signal charge of 1 e- to 20 e- arrives at the input. Preferably, the four MOSFET transistor cascode amplifier operates in open loop once the feedback MOSFET transistor is switched off by the input signal. Preferably, the output N-MOSFET discriminator transistor senses the voltage of the output node with its gate connected to the output node, its drain connected to an external current source, and its source connected to the ground. Preferably, an external voltage called V_{REF} controls the voltage of the output node of the cascode transconductance amplifier and determines the operating conditions of the output N-MOSFET discriminator transistor. Preferably, the voltage V_{REF} is chosen in such a way that the output MOSFET transistor is biased in the sub-threshold region (which is also termed weak inversion) and switches on when an input charge signal occurs thereby moving the output node of the discriminator transistor from the supply voltage VDD to ground. Preferably, the dimensions of the input P-MOSFET transistors are sized for minimum noise compared with the N-well diffusion capacitance, or the PIN amorphous Si:H diode capacitance.

The N-MOSFET transistors of the output current source are preferably dimensioned and laid out for minimum drain capacitance. Preferably, the parasitic capacitance between the input node and the output node of the amplifier is minimised in order to maximise the open loop gain of the amplifier branch. Preferably, the amplifier is biased with a low current to

keep the power consumption of the pixel cell below 250nW. Preferably, the readout circuit further includes a fast OR-line connecting together a group of pixels. The group of pixels forms a macropixel that is read out by the peripheral readout of the integrated circuit. Preferably, each macropixel has a driver circuit that interfaces with the readout of the end-of- column logic circuit.

In a further preferred embodiment, there is provided an analogue output for summing signals inside a macropixel. In another preferred embodiment, the invention is arranged to have high gain signal integration for very sensitive APS applications in which the reference current is controlled to perform a soft pixel reset without KTC reset noise.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG 1 is a circuit diagram illustrating the architecture of a typical prior art APS circuit;

FIG 2a is a schematic circuit diagram illustrating the basic principle of the architecture of an individual sensing device, such as a pixel cell, according to an embodiment of the invention;

FIG 2b is a schematic circuit diagram of an individual sensing device, such as a pixel cell, according to an embodiment of the invention in an open-loop condition with polarity inversion across a feedback transistor;

FIG 3 is a schematic circuit diagram illustrating the binary architecture circuit of an individual sensing device, such as a pixel cell, of the type shown in Figures 2a and 2b;

FIG 4 is a schematic circuit diagram of the binary readout architecture circuit for reading the outputs of a plurality of sensing devices, for example pixel cells, of the type shown in Figure 3;

FIG 5 is a graph of waveforms showing the transition from closed-loop to open-loop operation of the amplifier of Figures 2a, 2b and 3;

FIG 6 is a graph of waveforms of the input sensing node, output transconductance amplifier node and output of the transistor discriminator of the pixel shown in Figures 2a, 2b and 3 for input charges of 12.5 e-, 25 e-, 50 e- and 100 e-;

FIG 7 is a graph of the waveforms of the output transconductance amplifier node of the sensor, for example a pixel, shown in Figures 2a to 3 for an input charge of 75 e- and input current of 1pA, 2pA, 5pA, 10pA and 20pA;

FIG 8 is a graph of the variation of the source voltage with the drain current at a constant gate voltage of a feedback MOS transistor working in weak inversion as used in Figures 2a to 3;

FIG 9a is a graph of the noise calculation as function of the input-sensing node capacitance of the Single Particle Detection sensing device, such as a pixel cell, shown in Figures 2a to 3;

FIG 9b is a graph of the noise calculation as function of reference current of the SPD sensing device shown in Figures 2a to 3;

FIG 10 is a schematic diagram of the architecture circuit for a charge integrating device embodying the invention;

FIG 11 is a graph of the input current, one electron every 500ns, of the input node and of the output node of the integrating sensing device of Figure 10;

FIG 12 is a graph of the noise (ENC) as a function of the operating temperature, from 77K to 297K of the binary sensing device, for example pixel, circuit of Figure 3;

FIG 13 is a graph of the binary sensing device circuit of Figure 3 for 1.5fF sensor capacitance set to detect 3 electrons charge;

FIG 14 is a view of a macropixel arrangement grouping together 16 pixels of the type shown in Figure 3;

FIG 15 is a cross-section of a sensor ASIC assembly into which the pixel of Figures 2a to 4, and 10 may be diffused with an amorphous Si:H PIN sensor deposited on the surface of the ASIC;

FIG 16a is a block schematic diagram of an array of 64 pixels of the type shown in FIG 3;

FIG 16b is an array of 64 pixels of the type shown in Figure 3 arranged in an 8x8 matrix and forming a macropixel that may be read out with an analogue multiplexing APS readout scheme; and

FIG 17 is a large area sensor such as a complete wafer carrying an assembly of arrays of the type shown in Figures 4, 16a and 16b.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In Figure 2a there is shown a simplified schematic block diagram of one sensing device 10, such as a pixel cell, of a Single Particle Detector (SPD) plane array of many such devices, or cells, formed in an integrated circuit. The sensing device 10 comprises a sensor 12, such as a pixel sensor, a transconductance amplifier 14, a current mirror formed from two transistors T2 and T3, a feedback MOSFET transistor T1, and an output MOSFET transistor T4. The sensor 12 is connected to the input of the amplifier 14. The feedback MOSFET transistor T1 is connected between the input and the output of the amplifier 14 and the output of the amplifier 14 is fed to the output MOSFET discriminator transistor T4. The total capacitance C_f between the input node and the output node of the amplifier 14 comprises the sum of the parasitic capacitance between the input node and the output node and the drain-to-source capacitance of the feedback transistor T1 as shown in Fig 2a.

Each sensor 12 may be a pixel sensor comprising an N-well diffusion working in linear or avalanche regime, a PIN amorphous silicon sensor deposited onto the substrate, a p-n photodiode, an avalanche photodiode

integrated in the substrate, or a radiation sensor for detecting charged particles and/or X-ray photons.

An input current source I_{REF} 18 is mirrored by a current mirror comprising the diode-connected MOSFET transistor T3 and transistor T2.

In the embodiment illustrated in Figure 2a, the current source 18 (I_{REF}) injects the mirrored current via the MOSFET transistors T3 and T2 forming the current mirror, into the feedback MOSFET transistor T1. The typical range value of I_{REF} is between 1pA to 20pA biasing the feedback MOSFET transistor T1 deeply in weak inversion. The source of the feedback MOSFET transistor T1 causes the potential of the output V_{OUT} of the transconductance amplifier 14 to be governed by the gate voltage V_{REF}. The precise potential value of the output node is:

$$V_{OUT} = \frac{V_{REF}}{n} - \mathrm{U_T Log}\left[\frac{I_{REF}}{2n\mu C'_{ox} W/L U_T^{\,2}}\right]$$

The value of the reference voltage V_{REF} is chosen such that the output node is held at a potential V_{OUT} lower than the potential of the input node V_{IN} biasing the feedback MOSFET transistor T1 with its drain-to-source voltage positive and sufficient to operate it in saturation.

The DC input voltage V_{IN} is determined by the operating condition of the input MOSFET transistor (not shown) of the transconductance amplifier 14

and is typically the supply voltage VDD minus the gate-to-source voltage of a MOSFET transistor.

Each electromagnetic radiation quantum impinging on the substrate and epitaxial layer in the vicinity of the p-n junction formed by the sensor 12 which may be, for example, a pixel sensor comprising an N-well diffusion or a PIN amorphous Si:H diode (in the case of the amorphous-silicon-thin-film-above-integrated-circuit implementation) generates a packet of electron-hole pairs (typically 80 e^-h pairs for 1μm thick silicon layer). The electron charge packet ΔQ_{DET} then drifts by thermal diffusion, or by the electric field in the case of the amorphous-silicon-thin-film-above-integrated circuit implementation, and is collected by the sensor 12 which may be, for example, an N-well diffusion or a PIN amorphous Si:H diode, thereby building up a negative voltage step – ΔV_{IN} at the input of the transconductance amplifier 14 on top of its DC potential V_{IN}.

The voltage step ΔV_{IN} is $\frac{\Delta Q_{DET}}{C_{IN}}$, in which C_{IN} is the total input capacitance including all capacitances connected to the input sensing node, which is typically 2fF for a PIN amorphous Si:H diode to 3 - 5fF for a diode sensor in the bulk material (substrate). The input voltage step ΔV_{IN} generates an output current step ΔI_{OUT} at the output of the transconductance amplifier 14.

The current step is given by $\Delta I_{OUT} = -\,gm\,\Delta V_{IN}$.

The amplifier 14 works first as a transresistance amplifier and consequently the reference input current I_{REF} is mirrored in the feedback branch formed by the feedback MOSFET transistor T1. In the steady state, the feedback transistor T1 is connected in grounded gate configuration with the source as the output node and the drain as the input node.

At a hit by a particle or photon, the negative voltage step - ΔV_{IN} is built up at the input of the transconductance amplifier 14 which then generates an output current step at its output $\Delta I_{OUT} = -gm\ \Delta V_{IN}$. This current variation produces a rising voltage ΔV_{OUT}, which decreases the feedback current from its initial value I_{REF}, to a lower value depending on the ΔV_{IN} amplitude. If this ΔV_{IN} variation is sufficiently large, the drain current of the feedback MOSFET transistor T1 decreases to zero and the transconductance amplifier 14 starts to function in open-loop mode. If this variation ΔV_{IN} is small enough and the feedback drain current greater than zero, then the transconductance amplifier loop remains closed, and functions as a transresistance amplifier.

The current I_{REF} is set to keep the feedback transistor T1 in deep weak inversion giving an extremely low drain-to-source capacitance C_{DS} of around 5-20aF and thereby the sensitivity of a quantum device as shown in Fig. 2a. In deep submicron CMOS FETs such as the feedback transistor T1, which are of the order of 0.25μm, or smaller, and which are biased in deep weak inversion, the capacitance from drain-to-source tends to zero when the ground-to-source voltage is less than 0.4V. Under these conditions, the

feedback transistor T1 operates as a switch controlled by the input signal itself, needing no additional reset facility and hence there is no reset noise.

Figure 2b shows the sensing device, which is preferably a pixel cell, of Figure 2a in open-loop condition in which the source S and the drain D of T1 are interchanged compared to that shown in Figure 2a. The other elements of the sensing device shown in Figure 2b and the operation thereof are otherwise identical to that described above with regard to Figure 2a.

In the sensing device illustrated in Figure 2b, the threshold for the transition from closed-loop to open-loop occurs at a very small drain current of the feedback MOSFET transistor T1. When the output voltage variation of the output node of the transconductance amplifier 14 is large enough to invert the polarity of the drain-to-source voltage of the feedback MOSFET transistor T1, the drain swaps with source, as shown in Figure 2b. The source is then connected to the input sensing node and the gate-to-source voltage of the feedback MOSFET transistor T1, which is the reference voltage V_{REF} minus the input DC voltage of the transconductance amplifier 14, is constant during the polarity inversion time period.

The voltage reference V_{REF} is low enough that the gate-to-source voltage of the feedback MOSFET transistor T1 keeps its OFF-drain current, which is governed by:

$$I_{Doff} = 2n\mu C'_{ox} W/L U_T^2 e^{\frac{V_{REF} - n\Delta V_{INDC}}{nU_T}}$$

small enough to avoid discharging the input sensing node and the output node of the transconductance amplifier 14, as illustrated in Figure 2b.

Typically, the open-loop transition of the transconductance amplifier 14 and the drain-source polarity inversion of the feedback MOSFET transistor T1 occurs for input charges greater than 10 e-. In this operation mode the amplifier stage has a voltage gain defined by:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = -gm.R_{OUT}$$

For typical values of transconductance gm of 10^{-5}S, and output resistance R_{OUT} of the transconductance amplifier 14, of 10^8 to 10^9 ohms, typical open voltage gain $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$ is about 1000 to 10000. Therefore, a conversion gain of 5 to 10 mV/e- may be achieved which is a value that is 3 orders of magnitude larger than those of conventional APS pixel cells for which the output signal is the input signal ΔV_{IN} buffered by a source follower.

For this very high gain, the rise time of the output voltage at the transconductance output node is determined by the slew rate imposed by the output current of the transconductance amplifier 14, and not by the output time constant $R_{OUT}C_{OUT}$. The output voltage rise time is governed by the equation:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{qQ_{DET}}{nkTC_{OUT}C_{IN}} I_{BIAS}$$

I_{BIAS} is the bias current.

Response time Δt_R is determined by the minimum detectable voltage ΔV_{MIN} seen at the input of the transistor discriminator T4 is:

$$\Delta t_R = \Delta V_{MIN} \frac{nkTC_{OUT}C_{IN}}{qQ_{DET}I_{BIAS}}.$$

After an input charge event, the feedback loop remains open until the input current source 18 smoothly resets the input sensing node to its initial DC value with a time equal to about Q_{DET}/I_{REF}. For typical values of I_{REF} and ΔQ_{DET} of 10pA and 100 e-, the recovery time is about 1.6 microsecond. The time constant of the output node, which is shorter, is defined by $\tau_{OUT} = R_{OUT}C_{OUT}$. For $Rout = 10^8$ and $Cout = 1fF$, it is typically 100ns.

The value of the current reference I_{REF}, adjusted externally on the periphery of the chip, determines the threshold level that triggers the open loop regime.

The feedback MOSFET transistor T1, together with the input current source 18 (I_{REF}), provides the automatic DC control of the potential of the input sensing node, without the help of any additional reset device. The feedback MOSFET transistor T1, together with its associated diode-connected MOSFET transistor T3 of the current mirror T3 T2 which mirrors the current

I_{REF}, also provides the control of the non-linear operation of the amplifier 14 and determines the threshold of the open-loop operation.

The value of the voltage reference V_{REF}, adjusted externally on the periphery of the chip, determines the threshold level of the output MOSFET transistor T4 which acts as a discriminator transistor. During the occurrence of an input charge ΔQ_{DET}, the gate of the output MOSFET transistor T4 senses the positive signal voltage pulse ΔV_{OUT} generated at the output of the transconductance amplifier 14, and generates an output current that quickly lowers the output node from the positive supply rail to the ground level. The output MOSFET transistor T4 works in weak inversion, and with an appropriate value of V_{REF}, output transistor T4 works likes a discriminator, the exponential current I_{DO} rise playing the role of discrimination being governed by:

$$I_{DO} = 2n\mu C'_{OX} W/L U_T^{\,2} e^{\frac{V_{REF} - n\Delta V_{OUT}}{nU_T}}$$

For example, a DC drain current of transistor 30 set to 1nA by V_{REF}, and a output voltage swing ΔV_{OUT} 10 times U_T (250mV) raises the drain current 3 orders of magnitude to 1μA, which is sufficient to switch the output node fed down to ground level with an external current source set to 0.5μA.

The output MOSFET transistor T4 provides a fast signal discrimination function with a threshold value between $5U_T$ to $10U_T$ and it also provides a local line driver function in generating an output binary signal without

consuming power, except when the circuit is activated by the occurrence of an input charge ΔQ_{DET} above its threshold.

Figure 3 shows a binary implementation of the sensing device, preferably a pixel cell, according to a preferred embodiment of the invention. The sensing device comprises a sensor 12, which is preferably a pixel sensor, a transconductance amplifier comprising two transistors M1 and M4, a current source 18, a current mirror comprising two transistors M3 and M6, a feedback transistor M2, and an output stage comprising two transistors M10 and M8 for output X and M11 and M12 for output Y. The sensor 12 is connected to the input of the amplifier M1 M4. The current source 18 is connected to the node of the input of the amplifier M1 M4 and the sensor 12. The feedback transistor M2 is connected between the input and output of the amplifier M1 M4. The output of the amplifier M1 M4 is connected to the output stage M10 M8 and M11 M12. Constant current load to the output of the amplifier M1 M4 is provided by transistors M5, M7 and M9. The X output current is taken from the drain of M10 and the Y output current is taken from the drain of M12.

As illustrated in Figure 3, the output discriminator stage M10 M8 and M12 M11 of the sensing device consists of the cascode amplifier formed by the N-MOSFET transistors M8 M10 and M11 M12. The complete dynamic operation of the circuit of Figure 3 is identical to that described with regard to Figures 2a and 2b above, however, the sensor 12 is returned to a bias voltage V_s. When the sensor 12 is an amorphous Si:H PIN diode deposited on ASICS, V_s is typically in the region –10V to –300V. When the sensor 12 is a p-n diode junction diffused on a substrate, V_s is at ground.

The circuit of Figure 3 may also be modified for circuit compactness reasons by replacing cascoded current source M5 M9 with a simple current source and the discriminator transistors M8 M10 with a single discriminator transistor.

Specific implementation of the concept of this embodiment of the invention may be readily constructed by the skilled worker in light of the foregoing disclosure.

In another preferred embodiment, an analogue readout may be obtained by replacing the discriminator transistor with an output analogue buffer as illustrated in Figure 10.

The amplifier branch M1 M4 M5 M9 is biased with a drain current I_{BIAS} of about 200nA keeping power consumption at about 250nW for a power supply VDD set to 1.4V.

The feedback transistor consists of an N-MOSFET transistor M2 dimensioned closed to minimum size working in weak inversion and in the saturation region, and biased such that its drain is connected to the input node, and its source to the output node. The input current source formed by the P-MOSFET transistor M3 is biased at a drain current chosen between 1pA to 20pA by the current mirror M6. M3 injects the same current in the feedback transistor M2 that operates as a DC feedback of the amplifier branch M1 M4 M5 M9. M3 keeps the potential of the input-sensing node, which is the gate of the transistor M1, automatically at the value needed to

bias M1 to the drain current imposed by the cascode current source M5 M9 and provides the bias potential of the sensor.

Figure 4 shows a sensing array 400 comprising an array 300 of sensing devices, for example pixels, of the type shown in Figure 3 or a macropixel 290 (an array of pixels connected to act as a single sensor) connected in a matrix of m rows and n columns. The X output of each row is connected to the input of a sense amplifier-comparator 410, there being one sense amplifier-comparator associated with each row. Similarly, the Y outputs of the sensing devices, which may be pixels, in each column are connected to the input of a sense amplifier-comparator 410. The sense-amplifier-comparators connected to the X outputs and the sense-amplifier-comparators connected to the Y outputs asynchronously detect the presence of a hit on a sensing device, for example a pixel, by electromagnetic radiation or charged particles. The outputs of the sense amplifier-comparators 410 are encoded into a binary word in a thermometric-to-binary encoder 420 to give the X and Y addresses/co-ordinates of the sensing device (eg pixel) which has received the hit. The X and Y addresses/co-ordinates are then available off-chip in the form of two digital bytes.

Figure 5 is a graph of the waveform of the input and output node of the transconductance amplifier as applied at V_{out} of Figures 3 (and 10) at an input charge of 25 e^-. The waveforms show the transition from closed-loop to the open-loop operation as function of reference currents of 5pA, 10pA, 20pA, and 50pA, as simulated with SPICE ™ for a 0.25μm CMOS technology.

Figure 6 is a graph of the waveforms of the input-sensing node, output transconductance amplifier node and output of the transistor discriminator for input charges of 12 e-, 25 e-, 50 e- and 100 e-, as applied at V_{out} of Figures 3 (and 10), as simulated with SPICE ™ for a 0.25μm CMOS technology.

Figure 7 is a graph of the waveforms of the output transconductance amplifier node for an input charge of 50 e- and input current of 2pA, 5pA, 10pA, 20pA, and 50pA, as applied at V_{out} of Figures 3 (and 10), as simulated with SPICE ™ for a 0.25μm CMOS technology.

Figure 8 is a graph of the variation of the source voltage with the drain current at a constant gate voltage of an MOS feedback transistor working in weak inversion in the pixels shown in Figures 2a, 3 and 10.

Figure 9a is a graph of the noise calculation of the SPD pixel cell shown in Figures 2a to 3, and 10 as function of the input-sensing node capacitance.

Figure 9b is a graph of the noise calculation of the SPD pixel cell shown in Figures 2a to 4 as function of reference current.

In a further preferred embodiment, as shown in Figure 10, the integrating architecture circuit of an individual sensing device, for example a pixel cell, is illustrated for operation in standard APS imaging mode. This embodiment is applicable to conventional APS imagers where charges are sequentially integrated in sensing devices (eg pixel cells) and sequentially read out by column with an analogue multiplexer performing the readout operation.

The sensing device 100 of Figure 10 comprises a sensor 12, a transconductance amplifier comprising two transistors M1 M4, which, together with feedback MOSFET transistor M2, and an input current source 18, operates as a high gain voltage amplifier between the input sensing node and a transistor M13 which acts as a source follower. The sensing device 100 also comprises a current mirror comprising two transistors M3 and M6, and an output stage comprising two transistors M13 and M14. The sensor 12 is connected to the input of the amplifier M1 M4. The current source 18 is mirrored by the current mirror M6 M3 and M3 provides the input current of to the amplifier 14. The feedback transistor M2 is connected between the input and output of the amplifier M1 M4. The output of the amplifier M1 M4 is connected to the output stage M13 M14. Constant current load to the output of the amplifier M1 M4 is provided by transistors M5, M7 and M9. The output of the sensing device 100 is taken as a voltage from the source of one of the transistors M13 in the output stage. This is in contrast to the embodiment shown in Figure 3 in which the output current is taken from the drain of the transistor discriminator M8 in the output stage.

Feedback MOSFET transistor M2 is kept at a very low current, for example 1fA, that is, it is almost switched off, during the readout sequence and the integration of sensor charges into the input sensing node. The input-sensing node is floating during the integrating and readout time period.

During the integrating time period feedback MOSFET transistor M2 is OFF with an inverted polarity topology. A soft reset operation is sequentially performed by applying an input DC current to the input current source 18, of

the order of 10pA, which biases feedback MOSFET transistor M2 in non-inverted polarity, and closes the loop on the non-linear transresistance amplifier M1M4. The floating diffusion of the sensor is then reset for the closed-loop DC potential of transconductance amplifier M1M4 without introducing KTC reset noise.

Figure 11 is a graph of the input current, one electron for each pulse, every 0.5μs, to the input node and of the output node of the integrating pixel of Figure 10.

The operation of a sensing device, such as a pixel, of the type shown in Figures 2a, 3 and 10, at cryogenic temperature will also improve circuit performance, as illustrated in Figure 12 which shows noise calculation as function of temperature. Cryogenic operation also improves charge collection of electrons in the silicon sensor layer by increasing the carrier velocity and the minority carrier lifetime, increases the sensitivity of the non-liner amplifier, and improves operating conditions of avalanche photodiodes.

Figure 13 shows simulations of the binary pixel circuit illustrated in Figure 3 with a 1.5fF sensor capacitance and designed in 0.25μm CMOS operating at liquid nitrogen temperature with a detection capability of 3 e-.

Referring to Figure 14, this Figure shows an array of sixteen pixels 10 of the type illustrated, for example in Figure 3, forming a macropixel arrangement. The outputs of the plurality of pixel cells 10 are connected to a common high-speed bus 11, such as a Fast-OR bus line, to form a macro-pixel. The bus 11 also provides a current source to the output stages of the pixels 10.

The Fast-OR line is read out by a logic circuit that connects the OR signal to the peripheral end-of-logic column, as shown in Figure 4.

The sensing devices according to an embodiment of the invention may be pixel cells diffused into an ASIC silicon chip of the type shown in Figure 15 which comprises a substrate 200 and a passivation layer 210 on which are deposited metal contacts 215. A layer 218 of n-doped amorphous Si:H is deposited over the metal contacts 215. A layer of intrinsic amorphous Si:H 220 is deposited onto the n-doped amorphous Si:H layer 218 and preferably covers the whole substrate 200. A thin p-doped layer 240 may be diffused into the upper surface of the layer of intrinsic amorphous Si:H 220 and an electrode pattern 250 may be deposited over the p-doped layer 240. A preferred thickness of the amorphous hydrogenated silicon substrate 200 is 10 to 30 μm. The ASIC assembly has the typical thickness of a silicon wafer.

In another preferred embodiment of the invention, in which the sensing device is preferably a pixel sensor, an array of 64 pixels of the type shown in Figure 3 may be arranged to form a macropixel, as shown in Figures 16a and 16b. The macropixel 290 comprises an array of 64 pixels 300, each pixel 300 being connected to a bistable output circuit 310 which switches a current source into a common bus 320. The output of the bus 320 can then be multiplexed using a multiplexer 330 with the output of other similar arrays to build a large area detector. Once readout of the bus 320 is complete, the bistables 310 are reset.

Figure 17 shows a large area sensor 350, typically a complete wafer, carrying an assembly of arrays 300 of the type shown in Figure 16a.

As mentioned above, in the embodiments illustrated in Figures 16a, 16b and 17, each pixel output 301 is connected to a separate bistable 310, one being allocated for each pixel. The output of each bistable 310 controls a current source 315 which is connected to a local bus 320 connecting the pixels 300 to form a macropixel 290. When a hit generated by an X-Ray photon occurs, the bistable state of the bistable 310 connected to the pixel which has been hit switches to 1 and turns on the associated current source 315. Then, each time a hit occurs in the macropixel area, another bistable 310 will switch on adding a current level to the macropixel bus 320. Once the readout time is over, the macropixel currents are readout as in standard analogue readout schemes of APS architecture, by analogue multiplexing. Once the readout is finished, a global reset is applied to all pixel cells which switches back to zero the current level of the macropixel bus 320, and a next readout cycle can start again.

In binary schemes, such as that shown in Figure 4, the readout of individual pixels for pixel density of 1 million/cm^2 could cause serious problems. Furthermore, most of the medical applications need pixel dimensions of 50μm to 100μm, and not the 10μm pixel size of the pixels embodying the invention. The Applicant has appreciated that the aggregation of arrays of pixels to form a macropixel 290 is a novel and inventive solution. The macropixel 400 illustrated in Figure 17 is particularly useful in HEP and medical applications and comprises a plurality of arrays of macropixels 290 incorporated into a wafer 400.

An additional advantage of forming a macropixel as described above and illustrated in Figure 16a, 1b and 17 is that it is possible to build a large area detector that may be incorporated into a wafer 410, as shown in Figure 17. The wafer 410 may be 8 inches in diameter with a 14cm square detector formed by the arrays of pixels 290. In this preferred embodiment, an interconnecting level may be added on top of the processed wafer before the amorphous Si:H deposition.

A further advantage of this embodiment is that whilst process defects may be present, which may be due to non-100% yield, they are localized in one pixel thereby killing the functioning of that pixel, but not the macropixel itself. This results only in a loss of efficiency of the device but does not affect the ability of the device to perform its function. For an aggregation of 100 pixels of 10μm in a macropixel of 100μm, one defect in the macropixel area of 100μm would decrease the efficiency only by 1%. Thus, even if a pixel is faulty, the macropixel device is still operable, albeit with a slight decrease in efficiency.

While the invention has been described in detail by specific reference to preferred embodiments, it is understood that variations and modifications may be made without departing from the true spirit and scope of the invention. In particular, the supply voltage may be varied. Also, advances in the semiconductor industry will provide, in the future, deeper submicron technologies for which scaling rules should be applied to the invention described herein to benefit from smaller parasitic capacitance and obtain better circuit sensitivity and lower power consumption. Scaling of the very

deep submicron future CMOS technologies will increase circuit sensitivity of the invention that will make possible single electron signal amplification and discrimination.

Furthermore, it will be appreciated that the values given above in the description of preferred embodiments are based on idealised circuit operation during computer simulation and for a given deep submicron CMOS technology, and that therefore relatively minor variations will not substantially affect the operation of the circuits illustrated in the accompanying Figures 2a to 4, 10 and 16a.

In summary, the present invention is applicable to the field of solid state radiation sensors, monolithic integration of active pixel sensors (APS), and more specifically to the field of imaging and Single Photon Detection and Single Particle Detection (SPD). An Active Pixel Sensor (APS) signal processing circuit is described for covering multi-electron level signals delivered by a pixel radiation sensor integrated in a monolithic integrated circuit designed with commercial deep submicron CMOS technologies. The readout circuit is an Application Specific Integrated Circuit (ASIC) that performs fast signal amplification and fast signal discrimination with a 12 MOSFET transistor 250nW circuit cell that is associated with each pixel radiation sensor. Each pixel sensor consists either of a p-n junction built in the bulk of the silicon substrate or of a PIN diode built in a thin film of hydrogenated amorphous silicon deposited on the top of the ASIC. The readout pixel circuit provides a fast logic signal or a fast analogue signal each time a photon or a charged particle impinges on the radiation pad sensor. This is accomplished without any additional peripheral processing circuit.

Furthermore, one or more embodiments of the invention are capable of single particle detection (SPD), and effectively operate as a quantum device by detecting each incident quantum individually. The embodiments of the invention are very sensitive devices which are compact and operate at extremely low power.

A variant of the circuit works by integration as for standard APS, but with an internal pixel gain of about 1000. Several readout pixel circuits with their associated pixel sensors of typical size ranging from 5μm x 5μm to 30μm x 30μm can be grouped together via a single analogue or a digital bus line to form a macropixel dimensioned to fit the required space resolution and desired pixel shape. Each macropixel information, binary or analogue can be retrieved individually with a synchronous readout with addressable column logic or with asynchronous column logic, or with an analogue multiplexer like in standard CMOS APS imagers.

Having described the preferred embodiments of this invention, it will be now apparent to one of ordinary skill in the art that other embodiments incorporating the concept may be used. Therefore, the invention should not be limited to the disclosed embodiment, but rather should be limited only by the spirit and scope of the following appended claims.

- KTC noise, also termed reset noise is the noise associated with the reset operation in APS circuits, CMOS imagers and CCD devices. In reference to the Fig.1 Prior art, each time the readout cycle is completed the input sensing node of S, gate of M1 is reset by the transistor reset switch M2 to a reference voltage that is applied to the gate of M2. This operation generates a noise at the input sensing node, the gate of M1, equal to $v_n^2 = \frac{kT}{C_{IN}}$, where C_{IN} is the input capacitance. Vn increases when C_{IN} decreases. This causes serious problems in a high density APS pixel circuit. An embodiment of the present invention aims to solve this problem by aiming to eliminate reset noise.

- ENC (ENCp for parallel noise ENCs for series noise): Equivalent Noise Charge, it is the r.m.s. charge usually expressed in electron r.m.s. that should be applied at the input of the amplifying channel to obtain the same output noise caused by the internal physical noise sources of this amplifying channel. The ratio of the input signal/ENC gives the signal-to-noise ratio, a basic number of the channel sensitivity.

- $U_T = \frac{kT}{q}$ is the thermal voltage about 25.6 mV, here K is the Boltzman constant 1.381 10^{-23} Joule/Kelvin, T is the absolute temperature in Kelvin (300K for room T), q is the electronic charge 1.602 10^{-19} C

- Cox" is the unit capacitance of the gate oxide of the MOS transistor. Typically, it is 5fF/um^2 for quarter micron CMOS technology used for in an embodiment of the present invention.

- C'_{OX} is the gate oxide capacitance per unit area of the MOS transistor. It is 5fF/um^2 in the quarter micron CMOS technology used in a preferred embodiment of the present invention. The sign " ' " means a normalized unit.
- n is the slope factor of the MOS transistor equal to $n = 1 + \frac{\gamma}{2\sqrt{\Psi_o + V_P}}$ with the surface potential $\Psi_0 \approx 2\Phi_F + 3U_T$ where Φ_F is the fermi potential, and $\gamma = \sqrt{\frac{2q\varepsilon_{si}N_{SUB}}{C_{OX}'}}$ where N_{SUB} is the substrate doping concentration ε_{si} the silicon permittivity 1.04 10^{-11} F/m, and V_p is the pitch off voltage of the MOS transistor
- μ is the carrier mobility
- W is the gate width of the MOS transistor defined by design
- L is the gate length of the MOS transistor defined by design
- C_{OUT} is the output capacitance of the output node of a preferred embodiment of the present invention, at the interconnection of the input branch with the load branch.
- C_{IN} is the capacitance of the input sensing node
- V_T is the threshold voltage of the MOS transistor
- gm (also gmf and gmi) is the transconductance of the MOS transistor, gate transconductance in weak inversion is $gm = \frac{I_D}{nU_T}$, source transconductance is $gms = \frac{I_D}{U_T}$
- Tm is the pulse shaping peaking time of the amplifying channel

II. Glossary of terms and labeling of components in figures

T1 Feedback transistor in fig.2B

T2 Input current source in fig.2B

T3 Current mirror controlling T2 in fig.2B

T4 Discriminator transistor in fig.2B

M1 Input transistor in fig.3

M2 Feedback transistor in fig.3

M3 Input current source in fig.3

M4 Cascode transistor of the input branch in fig.3

M5 Load branch in fig.3

M6 Current mirror controlling input current source M3 in fig.3

M7 Cascode transistor of the output load branch in fig.3

M8 Discriminator transistor branch X

M9 Bias current mirror transistor of the load branch

M10 Cascode transistor branch X

M11 Discriminator transistor branch Y

M12 Cascode transistor branch Y

M13 is the output source follower transistor of Fig.10

M14 is the output current source of Fig10

- Pixel sensor cell 12 is the generic name for the four sensor types (a-Si:H P-I-N diode, P-N diffused junction, APD P-N diffused junction, and amorphous Selenium layer)

- Input sensing node , referring to Fig 3 Binary architecture, it consists of the common interconnection of N-electrode of the pixel sensor cell with drain of the input current source M3, gate of the input transistor M1, drain of the feedback transistor M2.
- Input branch is transistors M1-M4
- Load branch is transistors M5-M7
- Discriminator output branch X is transistor M8-M10
- Discriminator output branch Y is transistor M11-M12
- V_{REF} Reference Voltage in Fig.2a, Fig.2b and Fig3 defines the operating point of the output branches X and Y
- I_{REF} is the reference current in Fig.2a, Fig.2b and Fig 3
- I_{BIAS} is the Bias current of the bias input branch and load branch via the mirror transistor M9
- Q_{DET} is the input charge generated by a particle hit in the pixel sensor cell.
- I_{DO} is the standing current in the input branch and load branch almost equal to the bias current (mirror current).

CLAIMS

1. A sensing device comprising a sensor for detecting arrival of an incident quantum of electromagnetic radiation and/or charged particles, and an amplifier connected to the sensor for amplifying a signal from the sensor, wherein the sensor and the amplifier are fabricated on a common substrate, the sensing device being arranged to discriminate between the arrival of single or multiple incident quanta at the sensing device.

2. A sensing device according to claim 1, wherein the sensing device is a pixel cell.

3. A sensing device according to any preceding claim, wherein the substrate comprises a monolithic semiconductor integrated circuit substrate.

4. A sensing device according to any preceding claim, wherein the sensor comprises a p-n junction sensor overlaying the substrate.

5. A sensing device according to any of claims 1, 2 or 3, wherein the sensor comprises a p-n photodiode.

6. A sensing device according to any of claims 1, 2 or 3, wherein the sensor comprises an avalanche photodiode integrated in the substrate.

7. A sensing device according to any of claims 1, 2 or 3, wherein the sensor comprises a radiation sensor for detecting charged particles and/or X-ray photons.

8. A sensing device according to any preceding claim, wherein the substrate comprises a silicon crystal bulk into which the sensor and amplifier are introduced.

9. A sensing device according to any preceding claim, further comprising an amorphous Si:H PIN diode having a plurality of amorphous Si:H layers

comprising an N doped layer, an Intrinsic layer, and a P doped layer, the layers being deposited above the substrate.

10. A sensing device according to any of claims 1 to 8, further comprising an amorphous selenium layer, the amorphous selenium layer being deposited above the substrate.

11. A sensing device according to any preceding claim, wherein the amplifier comprises a non-linear transresistance amplifier.

12. A sensing device according to any preceding claim, wherein the sensor and the amplifier are diffused onto the substrate.

13. A sensing device according to any preceding claim, wherein the sensor and the amplifier are deposited onto the substrate.

14. A device for producing a signal corresponding to a detection event comprising one or more of the sensing devices according to any preceding claim, further comprising a readout circuit for receiving the output of one or more of the sensing devices and producing an output signal corresponding to the detection event.

15. A device according to claim 14, further comprising a detection plane array of the sensing devices according to any of claims 1 to 13.

16. A device according to any of claims 14 or 15, wherein the readout circuit is a complementary metal oxide semiconductor (CMOS) circuit formed on the substrate.

17. A device according to claim 16, wherein the substrate is of a first conductivity type, the CMOS circuit comprising one or more metal oxide field effect transistors of a first conductivity type, a well region of a second conductivity type in said substrate, and one or more metal oxide semiconductor transistors of a second conductivity type formed in the well region.

18. A device according to any of claims 14 to 17, wherein the readout circuit comprises a first section and a second section.

19. A device according to claim 18, wherein the first section comprises a non-linear transresistance amplifier.

20. A device according to claim 19, wherein the non-linear transresistance amplifier comprises a transconductance amplifier, a feedback field effect transistor, and an input current source.

21. A device according to any of claims 18 to 20, wherein the second section comprises a transistor discriminator for generating a binary signal for each quantum of electromagnetic energy and/or charged particle detected.

22. A device according to any of claims 14 to 21, wherein the device is arranged to detect each quantum impinging upon each sensing device in Single Particle Detection (SPD) mode.

23. A device according to any of claims 14 to 22, wherein the device is arranged to integrate charges and sequentially reading the charges out in standard APS operation mode.

24. A device according to claim 20, wherein the sensor is a p-n sensor or p-i-n sensor, and the amplifier has an input sensing node, the input sensing node being connected to the drain of the feedback field effect transistor, the electrode of the sensor and the drain of the input current source.

25. A device according to any of claims 14 to 24, wherein the readout circuit has an output current, and the readout circuit is arranged to receive external reference signals, the external reference signals comprising a Voltage Reference, a Current Reference, and a Bias Current, wherein the external reference signals and the output current from the readout circuit are common to the one or more sensing devices.

26. A device according to any of claims 20 or 24, wherein the feedback field effect transistor has its source connected to the output of the transconductance amplifier.

27. A device according to claim 20, 24 or 26, wherein the feedback field effect transistor is arranged such that the feedback field effect transistor has a drain current equal to a reference current mirrored by the input current source when the feedback field effect transistor is biased in weak inversion, the field effect transistor forming the input current source, and the feedback field effect transistor DC biasing the sensor.

28. A device according to claim 20, 24, 26, or 27, wherein the feedback field effect transistor is arranged such that when biased at a low current between around 1-20pA the current decreases when an input signal occurs at the input sensing node by a particle or photon impinging on the p-n or p-i-n sensor.

29. A device according to claim 20, 24, 26, 27, or 28, wherein the transconductance amplifier is in closed-loop when said feedback field effect transistor operates as a feedback network and has a drain current above zero.

30. A device according to claim 29, wherein the transconductance amplifier is arranged to operate like a transresistance stage with the feedback field effect transistor operating as a feedback network.

31. A device according to claim 20, 24, 26, 27, or 28, wherein the feedback field effect transistor is arranged such that when the feedback field effect transistor turns off for an input signal charge above a threshold value the feedback field effect transistor has a drain current of about zero.

32. A device according to any of claims 14 to 31, wherein the quantum provides an input charge to the sensor, wherein the input charge is around 10 to 15 e- at a reference current of around 10pA.

33. A device according to any of claims 20, 24, and 26 to 31, wherein the non-linear transresistance amplifier is arranged to be in open loop when the feedback field effect transistor turns off for an input signal above threshold.

34. A device according to claim 20 or 33, wherein the non-linear transresistance amplifier has a low gain for small input signals below threshold when the feedback transistor is turned on, and the non-linear transresistance amplifier has a large gain for signals above threshold when the feedback transistor is turned off.

35. A device according to claim 21, wherein the discriminator transistor has its gate connected to the output of the amplifier, and its drain connected to the output of the sensing device, the output port of the sensing device being connected to the output signal, the output signal being a current.

36. A device according to claim 20, wherein the readout circuit is arranged to receive a Voltage Reference, the Voltage Reference establishing the voltage of the output node of the transconductance amplifier through gate-to-source voltage of the feedback transistor.

37. A device according to claim 36 wherein the voltage reference is arranged to bias the transistor discriminator in weak inversion at a drain current of few nanoamps.

38. A device according to any preceding claim, wherein the quantum impinges on one or more of the sensing devices generating a voltage across the sensor forming an input sensing node voltage, the input sensing node voltage decreasing and output voltage of the transconductance amplifier increasing when the quantum impinges on one or more of the sensing devices.

39. A device according to claim 21, 35 or 37, wherein the device is arranged such that when a voltage increases of the output node of the

transconductance amplifier occurs, the drain current of the discriminator transistor increases as the exponential of the voltage variation of the output voltage of the transconductance amplifier.

40. A device according to claim 39, wherein the drain current increase of the discriminator transistor is 1000 times (3 current decades) its value between around 1nA to 1μA for an output voltage increase of the transconductance amplifier of about 250 mV.

41. A device according to claim 21, 35, 39, or 40, wherein the current drain increase of the transistor discriminator switches the voltage of the output port of the sensing device and generates a binary signal.

42. A device according to claim 40, wherein an output voltage increase of about 250 mV is generated by an input charge of about 25 e^-.

43. A device according to any of claims 21, 35, or 39 to 42, wherein the readout circuit is arranged to receive a Voltage Reference giving a Voltage Reference value, the Voltage Reference value determining the standby current of the discriminator transistor to provide a discrimination threshold of the readout circuit.

44. A device according to any preceding claim, wherein the readout circuit comprises an integrating active pixel sensor (APS) imager.

45. A device according to claim 44, wherein the integrating imager includes a source follower stage in place of a discriminator transistor.

46. A device according to claim 44, or 45, wherein the integrating imager has an input current source, the input current source being switched off during integrating time and readout time.

47. A device according to claim 46, wherein the input current source is periodically biased at about 10pA during the reset time.

48. A device according to any of claims 17, 21, 23, 28, 30 or 31, wherein the device is arranged such that the feedback transistor switches off when the input signal rises above threshold to open the loop around the amplifier to cause a large increase in gain of the amplifier and thereby heighten the sensitivity of the one or more sensing devices.

49. A device according to any preceding claim, wherein the amplifier comprises a non-linear amplifier having an output and an input, the amplifier being arranged to have a feedback capacitance minimised to around 10^{-17} F for obtaining a charge-to-voltage conversion gain of about 5mV to 10mV at its output for each electron entering its input.

50. A device according to any of claims 14 to 49, wherein the device is an imaging device for producing an output signal corresponding to a detected image.

51. A macropixel comprising an array of sensing devices according to any of claims 1 to 13, wherein the outputs of said sensing devices are commoned to give the effect of a larger pixel.

52. A macropixel according to claim 51 wherein the outputs of the sensing devices are connected to a bus.

53. A macropixel according to claim 51 or 52, wherein the macropixel is configured such that if a sensing device in the macropixel should fail, the macropixel will continue to be operable but at a reduced sensitivity.

54. An array of macropixels according to any of claims 51 to 53 connected to detect an image.

55. A device comprising an array of macropixels according to claim 54, wherein the device is diffused into or deposited onto the surface of a wafer.

53. A sensing device substantially as hereinbefore described with reference to any one embodiment as that embodiment is illustrated in the accompanying drawings.

54. A macropixel substantially as hereinbefore described with reference to any one embodiment as that embodiment is illustrated in the accompanying drawings.

56. An array of macropixels substantially as hereinbefore described with reference to any one embodiment as that embodiment is illustrated in the accompanying drawings.

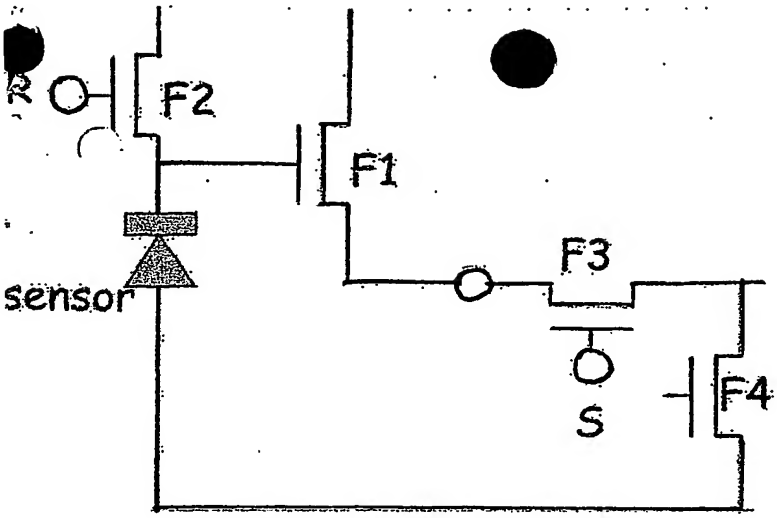
57. An imaging device substantially as hereinbefore described with reference to any one embodiment as that embodiment is illustrated in the accompanying drawings.

ABSTRACT

A Sensing and Imaging Device

A sensing device (10) comprises a sensor (12) for detecting arrival of an incident quantum of electromagnet radiation and/or charged particles, and an amplifier (14) connected to the sensor (12) for amplifying a signal from the sensor. The sensor (12) and the amplifier (14) are fabricated on a common substrate. The sensing device (10) is arranged to discriminate between the arrival of single or multiple incident quanta at the sensing device.

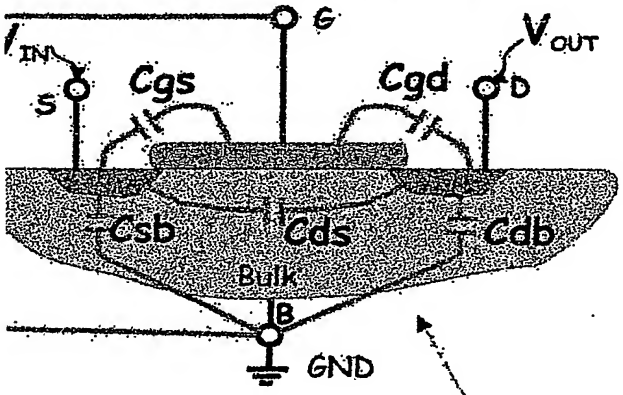
Figure 2a



F1 input source follower transistor
F2 Reset transistor
F3 pixel Select transistor
F4 Load
R Reset
S Pixel Select

Figure 1 Prior Art

pacitances of Feedback transistor T1



- Cds goes to 0 when Vgs goes to 0
- T1 is grounded gate
- overlap capacitances Cgd and Cgs are grounded
- total capaitance between D and S goes to 0 when Vgs < 0.4V

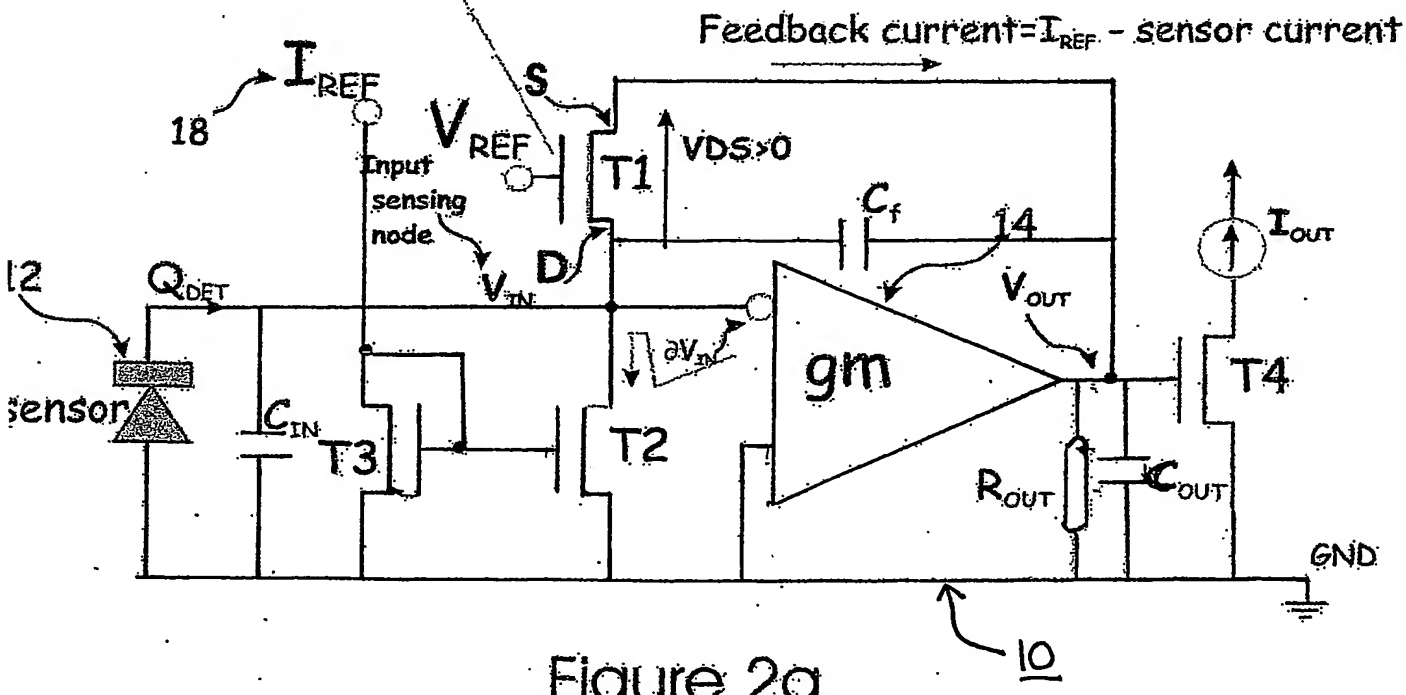


Figure 2a

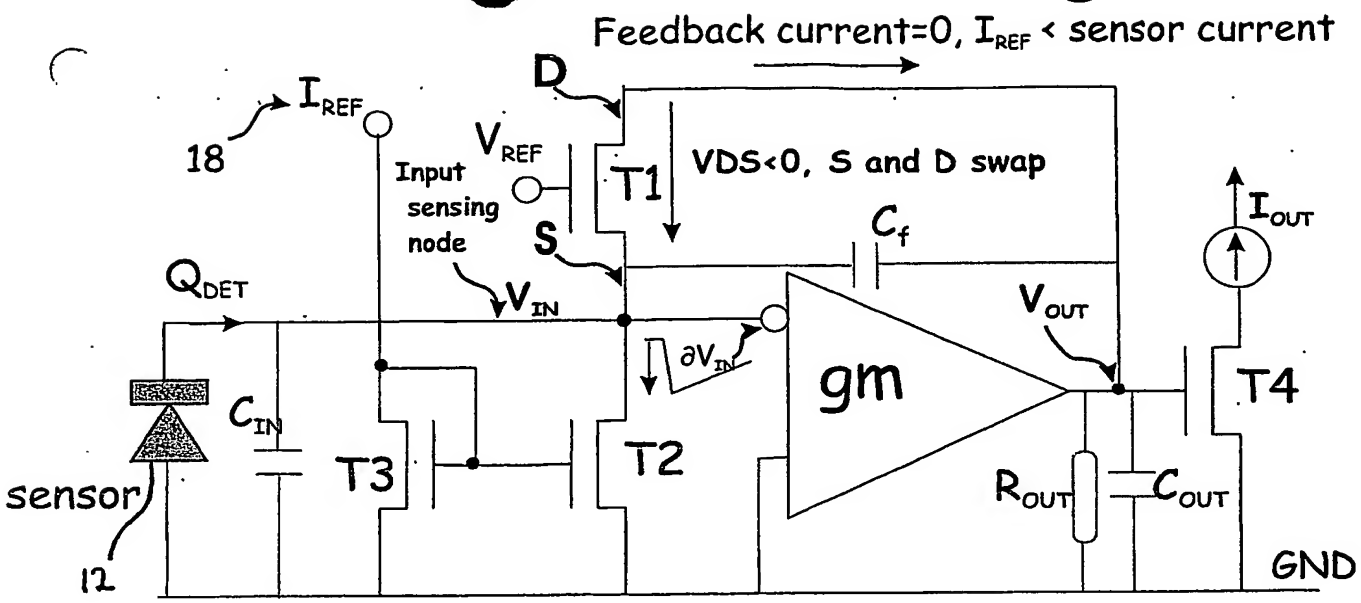
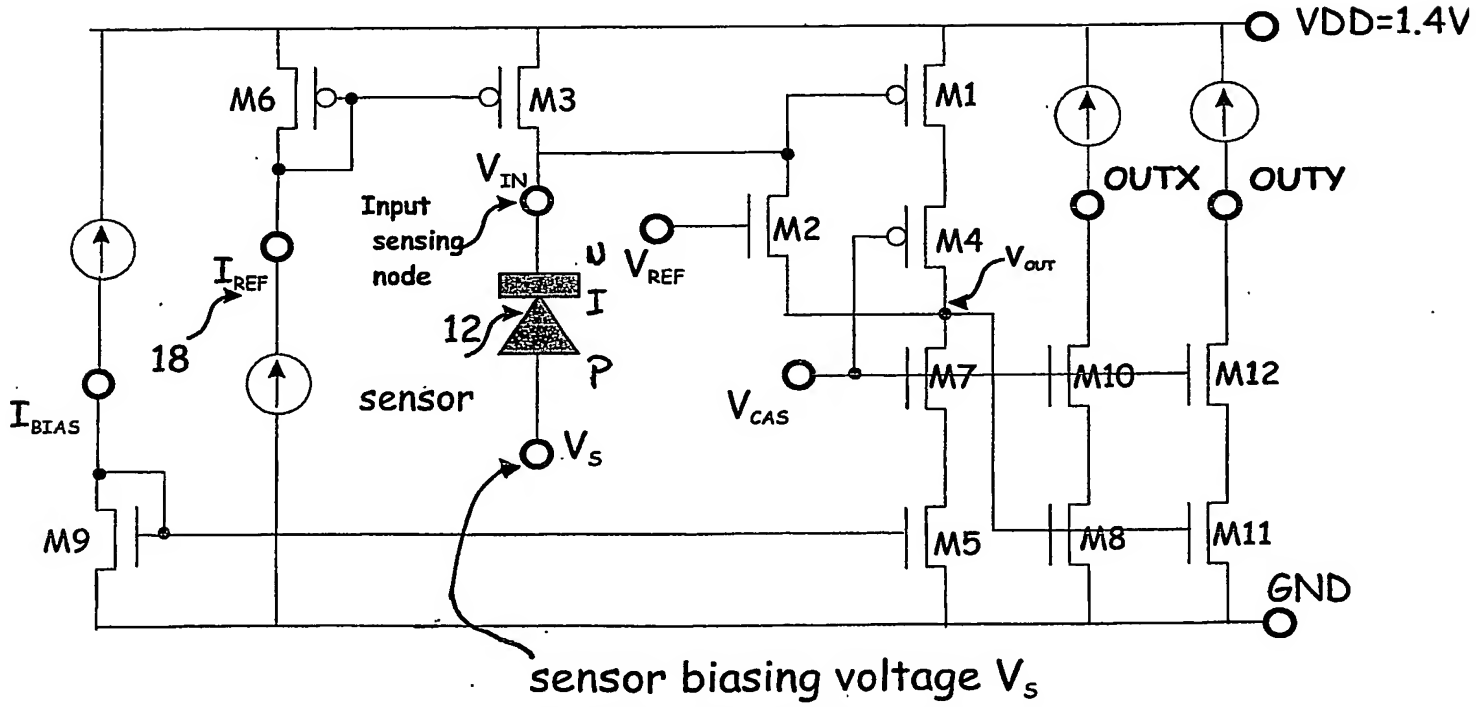


Figure 2b



- a-Si:H P.I.N. diode deposited on ASICs: V_S=-V_{BIAS}=-10V to -300V
- p-n diode junction Diffused on substrate :V_S=GND

Figure 3

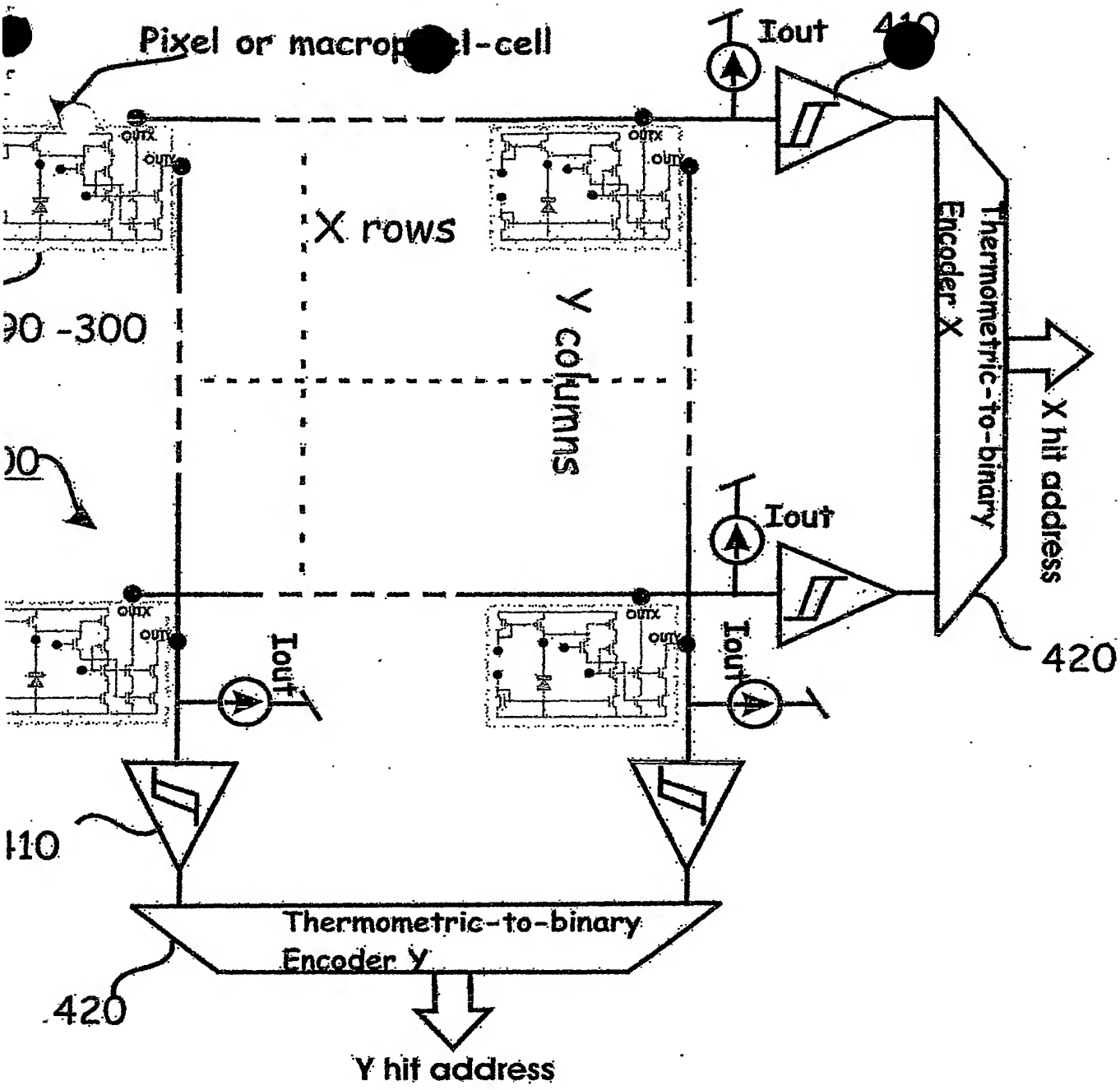
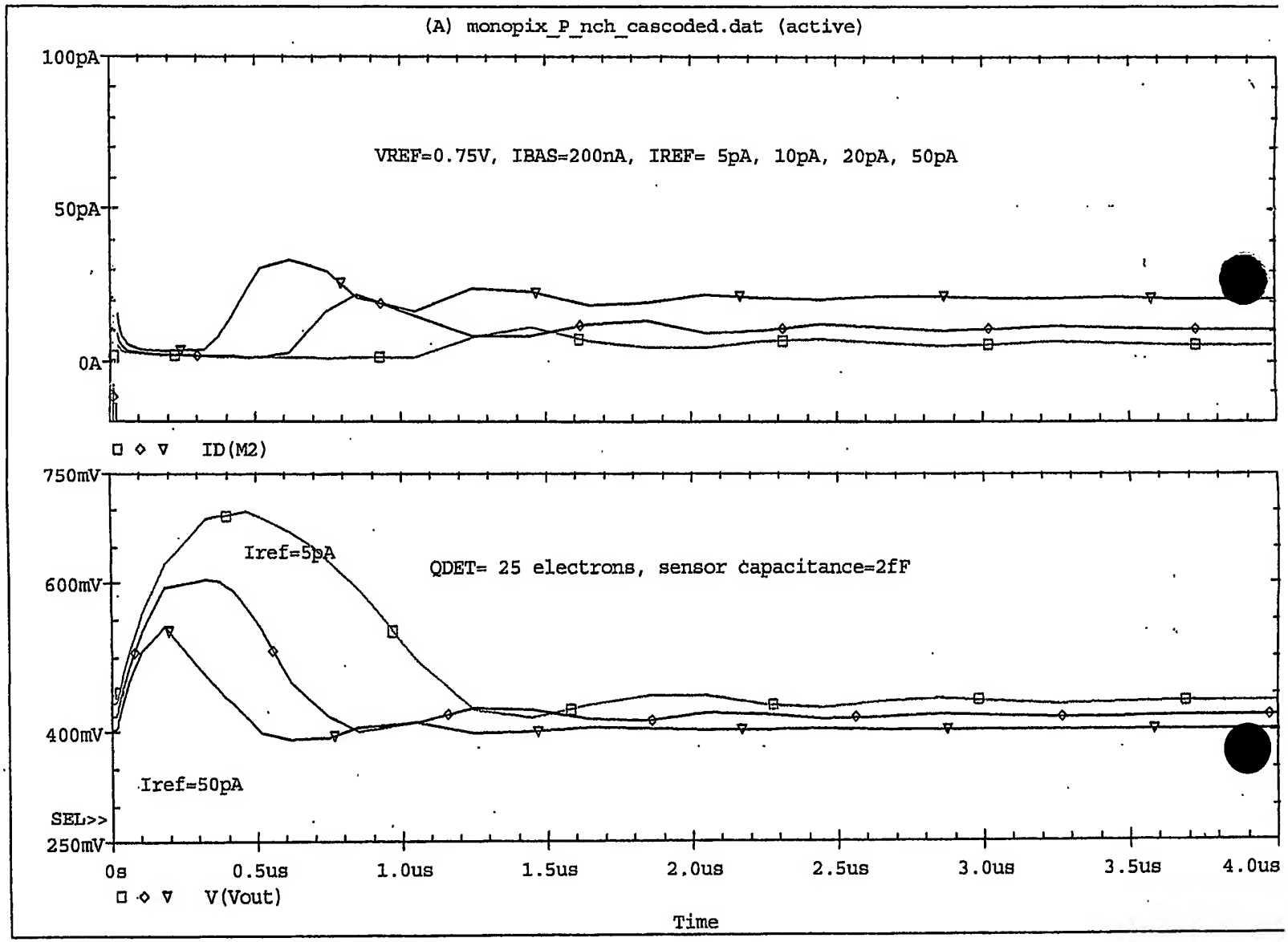
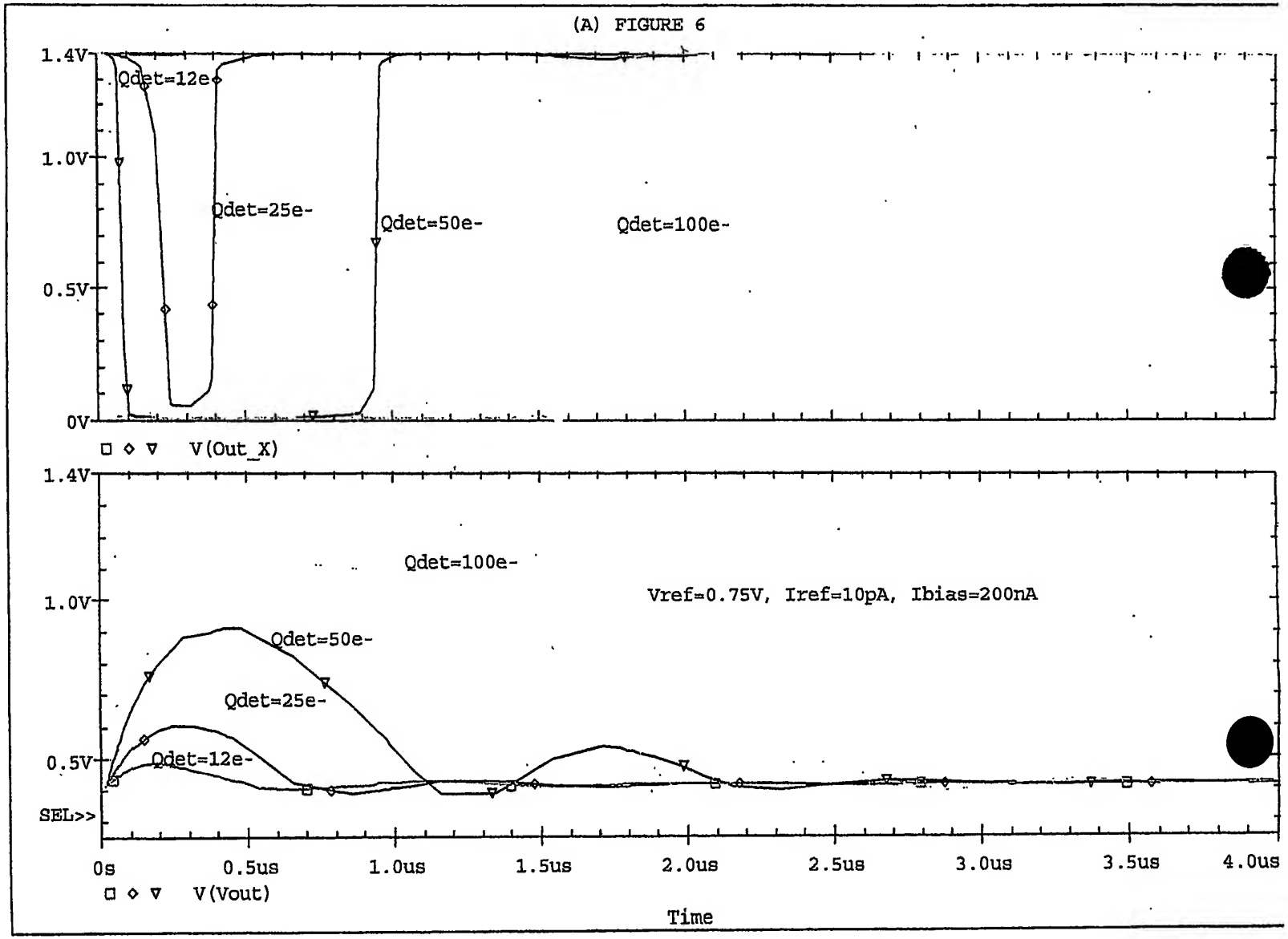

Pixel or macropixel-cell
Iout
X rows
Y columns
Thermometric-to-binary Encoder X
X hit address
420
Iout
Iout
Iout
Thermometric-to-binary Encoder Y
420
Y hit address

Figure 4

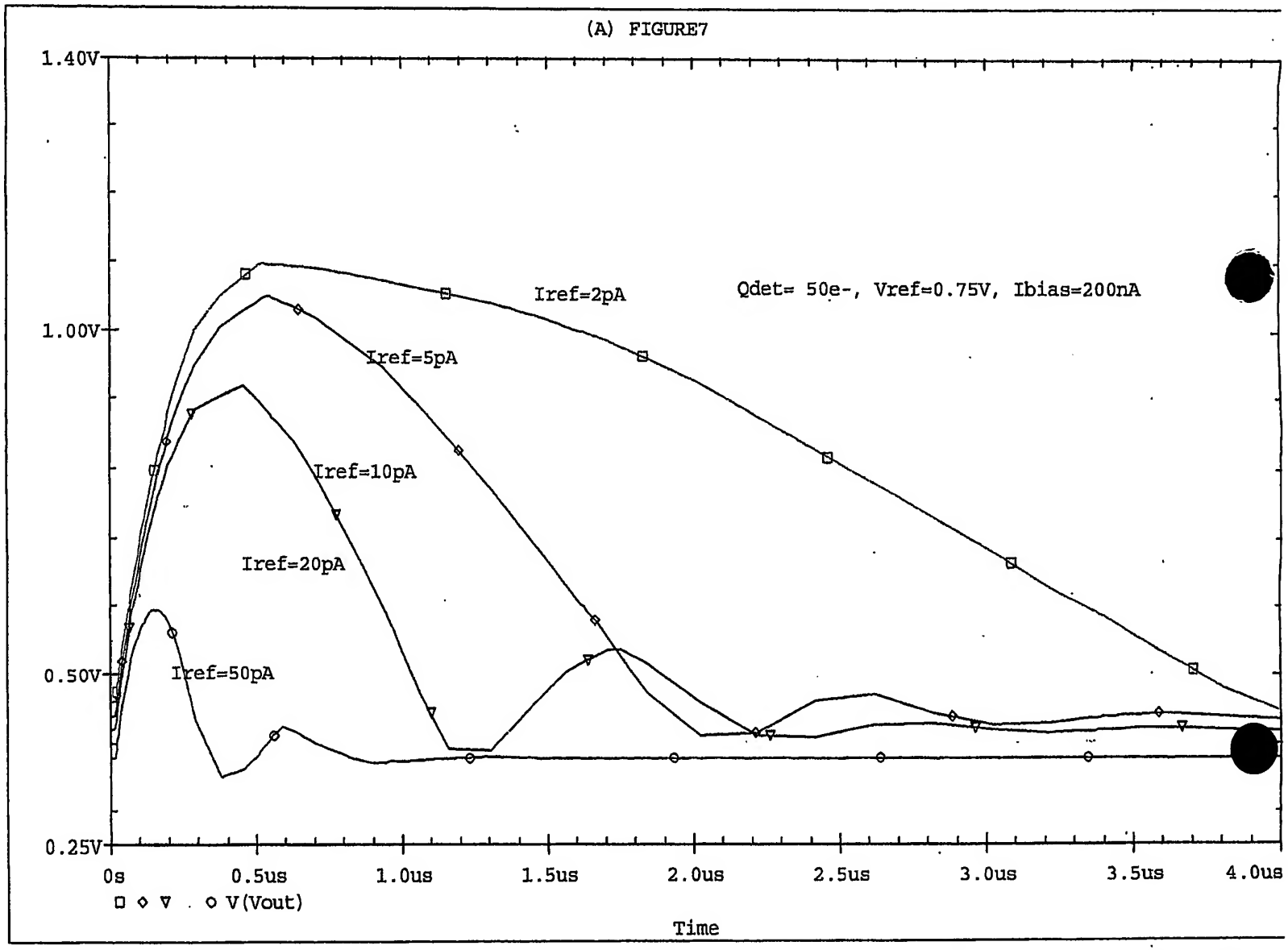
FIGURE 5


* \\cernhome04\jarron\PSPICE\Files\monopix_P_nch_cascoded.sch
Date/Time run: 11/27/01 11:44:52
Temperature: 27.
(A) monopix_P_nch_cascoded.dat (active)
100pA
50pA
0A
VREF=0.75V, IBAS=200nA, IREF= 5pA, 10pA, 20pA, 50pA
ID(M2)
750mV
600mV
400mV
250mV
SEL>>
Iref=5pA
Iref=50pA
QDET= 25 electrons, sensor capacitance=2fF
0s
0.5us
1.0us
1.5us
2.0us
2.5us
3.0us
3.5us
4.0us
V(Vout)
Time
Date: November 27, 2001
Page 1
Time: 12:03:0


(A) FIGURE 6
1.4V
1.0V
0.5V
0V
Qdet=12e
Qdet=25e-
Qdet=50e-
Qdet=100e-
V(Out_X)
1.4V
1.0V
0.5V
SEL>>
Qdet=100e-
Vref=0.75V, Iref=10pA, Ibias=200nA
Qdet=50e-
Qdet=25e-
Qdet=12e-
0s
0.5us
1.0us
1.5us
2.0us
2.5us
3.0us
3.5us
4.0us
V(Vout)
Time

* \\cernhome04\jarron\PSPICE\Files\monopix_P_nch_cascoded.sch

Date/Time run: 11/27/01 15:16:18 Temperature: 27.



Date: November 27, 2001 Page 1 Time: 15:20:3

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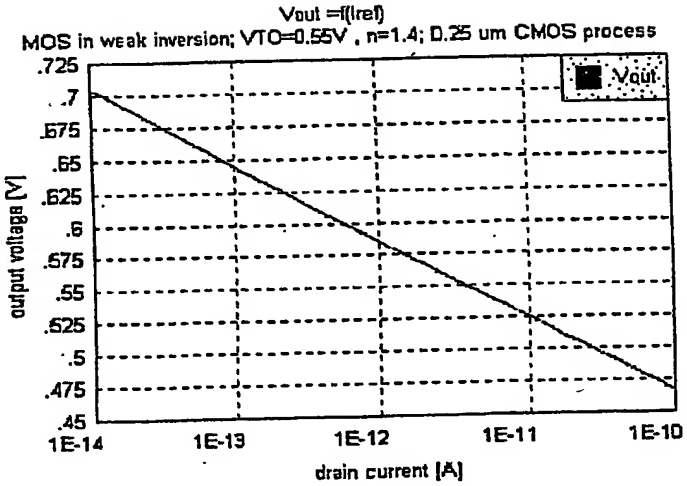
$$Iref = Io \cdot e^{\left[\frac{Vp - Vout}{Ut}\right]}$$

$$Io = 2 \cdot n \cdot Cox \cdot \left[\frac{W}{L}\right] \cdot Ut^2$$

$$Vp = \frac{Vref - Vto}{n}$$

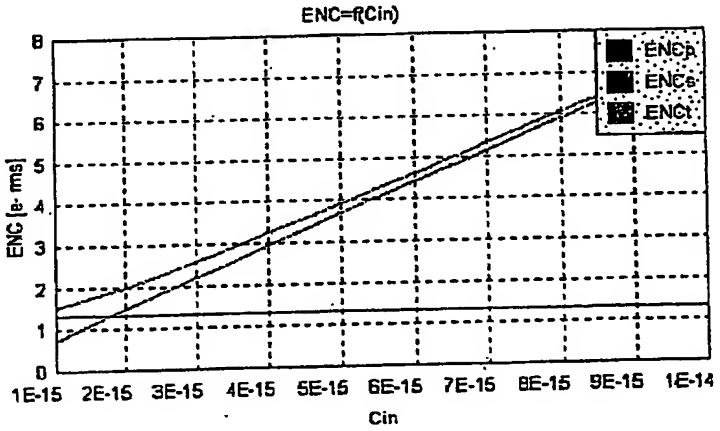
Figure 8



$$ENCt = \sqrt{ENCp^2 + ENCs^2}$$

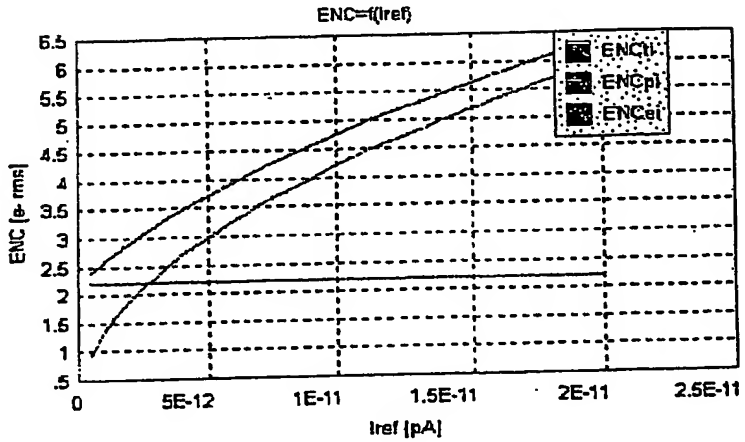
$$ENCs = \left[\frac{1}{q}\right] \cdot \sqrt{\frac{2 \cdot k \cdot T \cdot Cin^2 \cdot n}{gm \cdot Tm}}$$

Figure 9a



$$ENCp = \left[\frac{1}{q}\right] \cdot \sqrt{2 \cdot k \cdot T \cdot (gmf + gmi) \cdot Tm}$$

Figure 9b



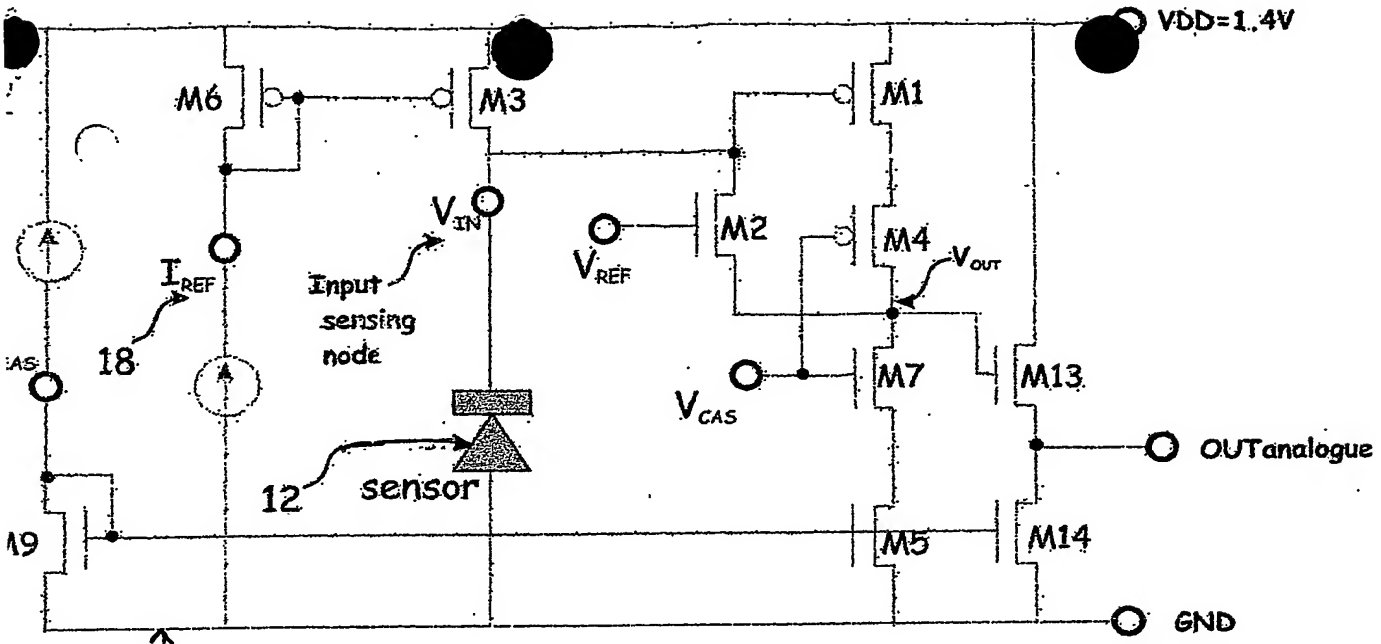
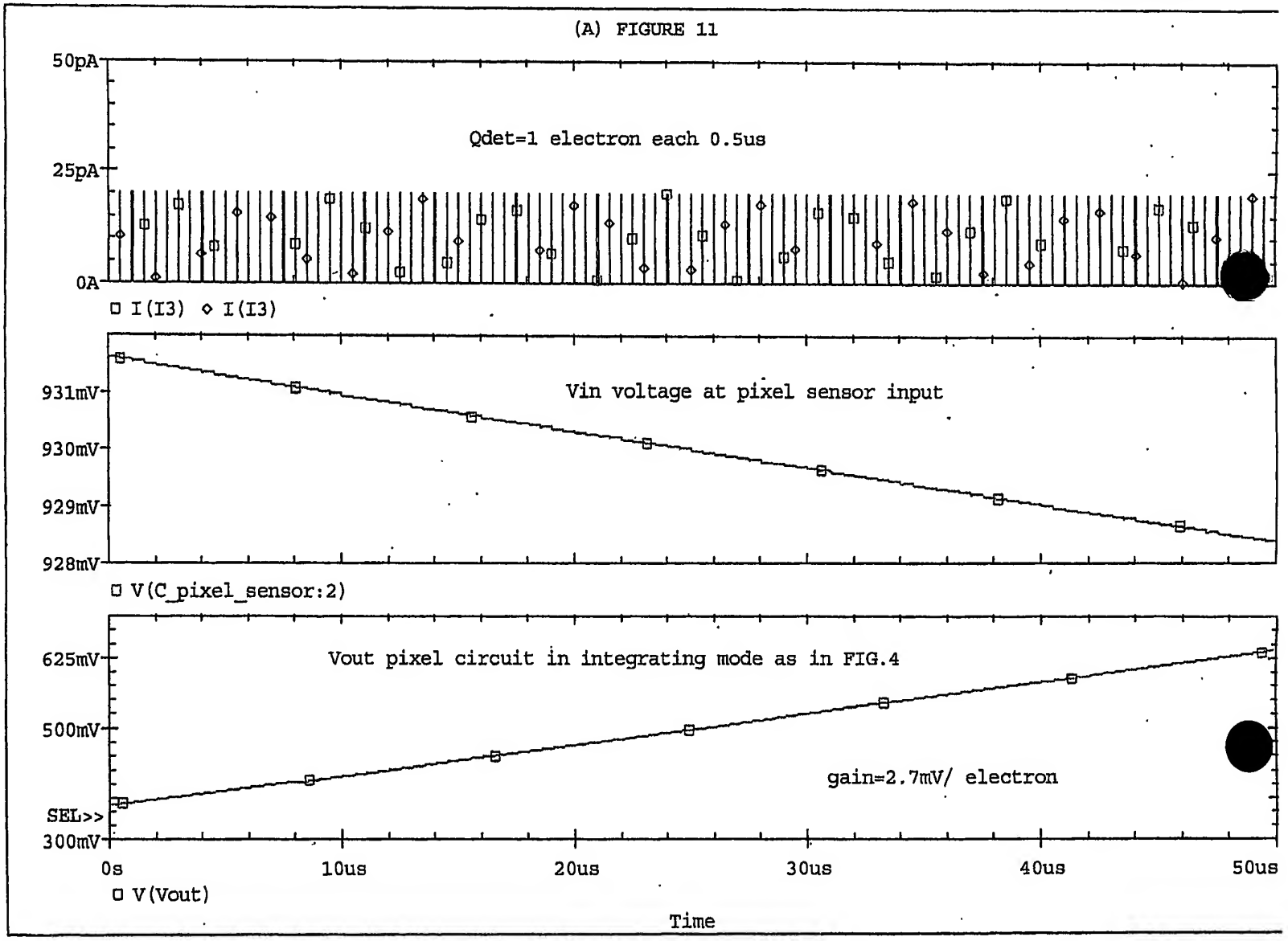

VDD=1.4V
M6
M3
M1
V_{IN}
V_{REF}
M2
M4
V_{OUT}
I_{REF}
Input
sensing
node
18
V_{CAS}
M7
M13
OUTanalogue
12
sensor
M5
M14
GND
100

Figure 10

* \\cernhome04\jarron\PSPICE\Files\monopix_P_nch_cascoded.sch

Date/Time run: 11/27/01 15:38:41 Temperature: -50.



Date: November 27, 2001 Page 1 Time: 15:57:2

9/14

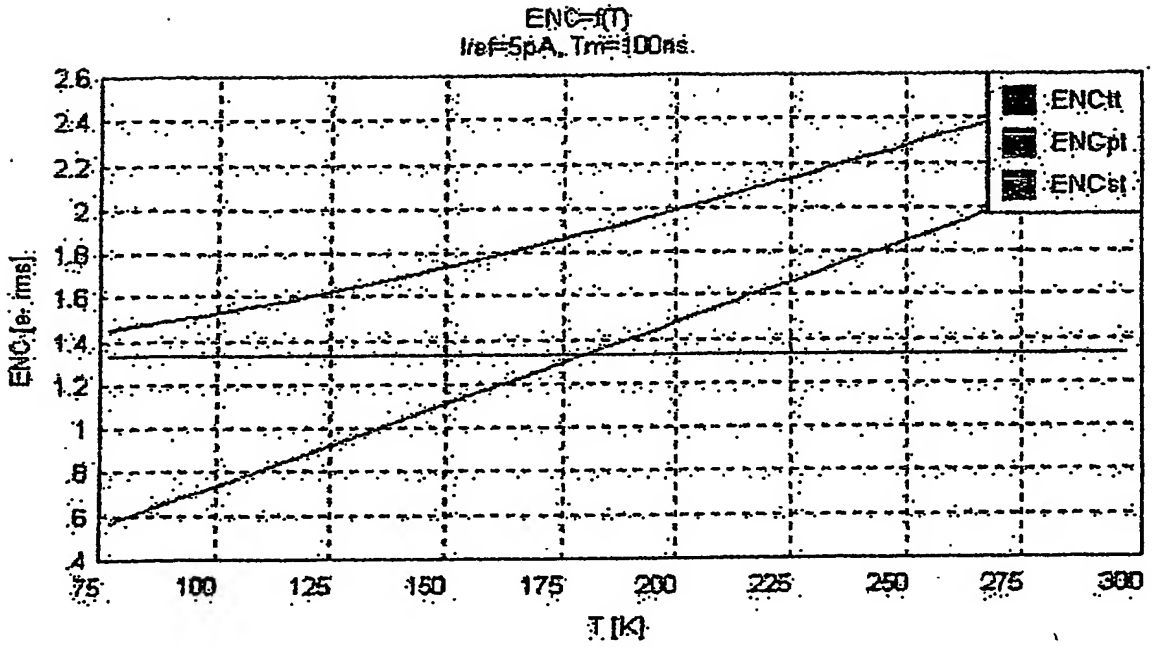
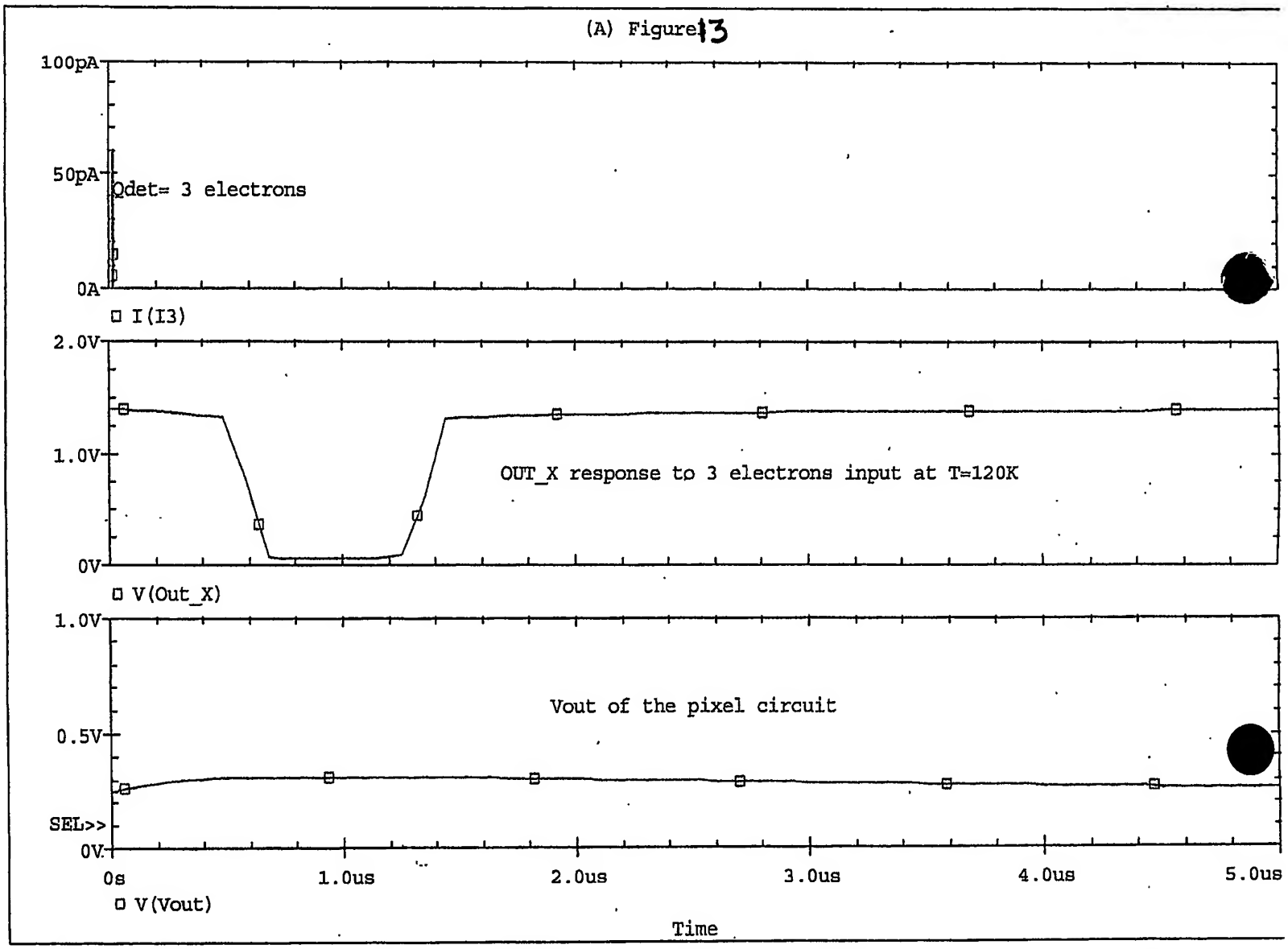

ENC=f(T)
Iref=5pA, Tm=100ns.
ENCtt
ENCpl
ENCsl
ENC [e- rms]
T [K]
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
.8
.6
.4
75
100
125
150
175
200
225
250
275
300

Figure 12

* \\cernhome04\jarron\PSPICE\Files\monopix_P_nch_cascoded.sch

Date/Time run: 11/27/01 16:22:18 Temperature: -150



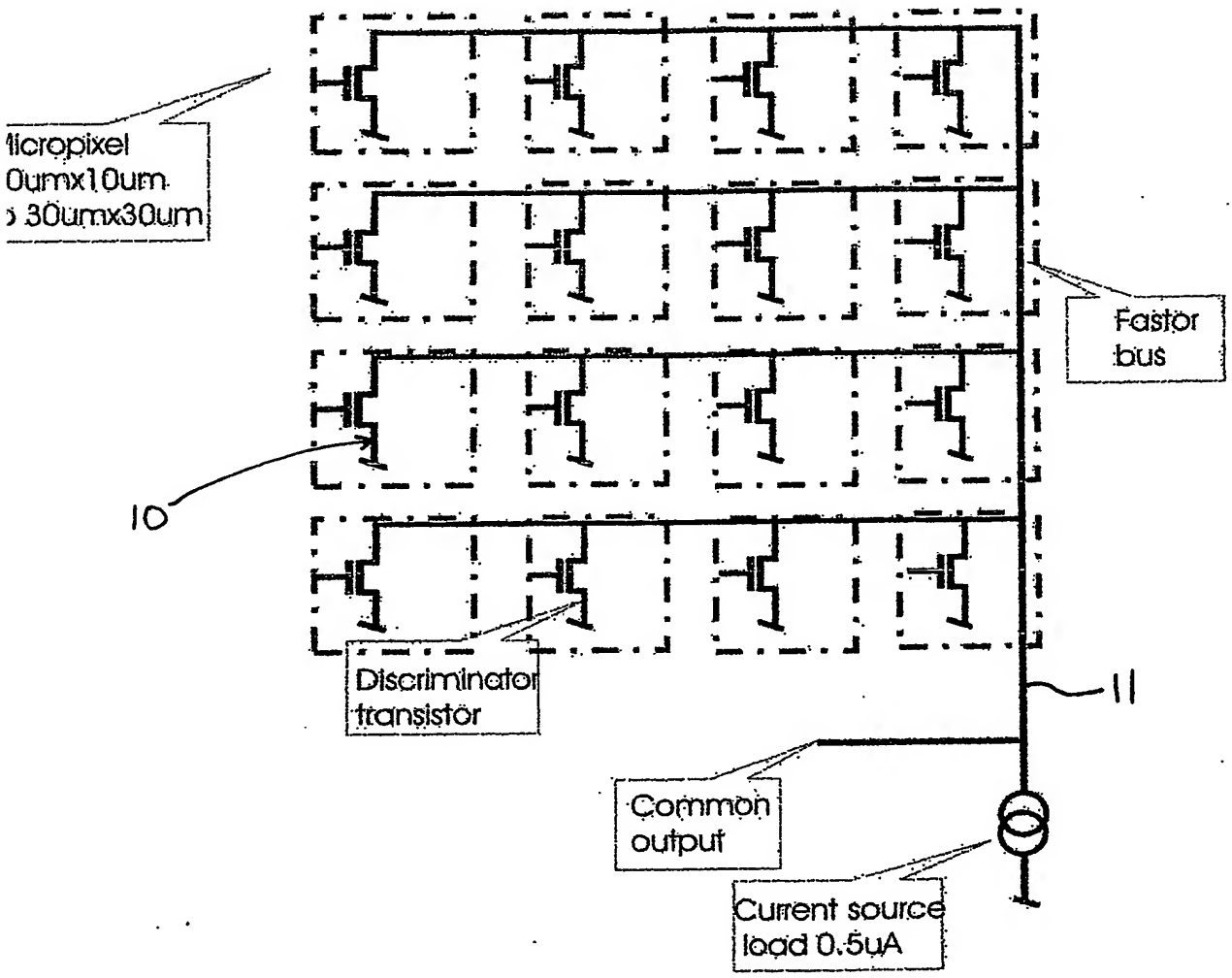

Micropixel
10umx10um
to 30umx30um
10
Discriminator
transistor
Faster
bus
11
Common
output
Current source
load 0.5uA

Figure 14

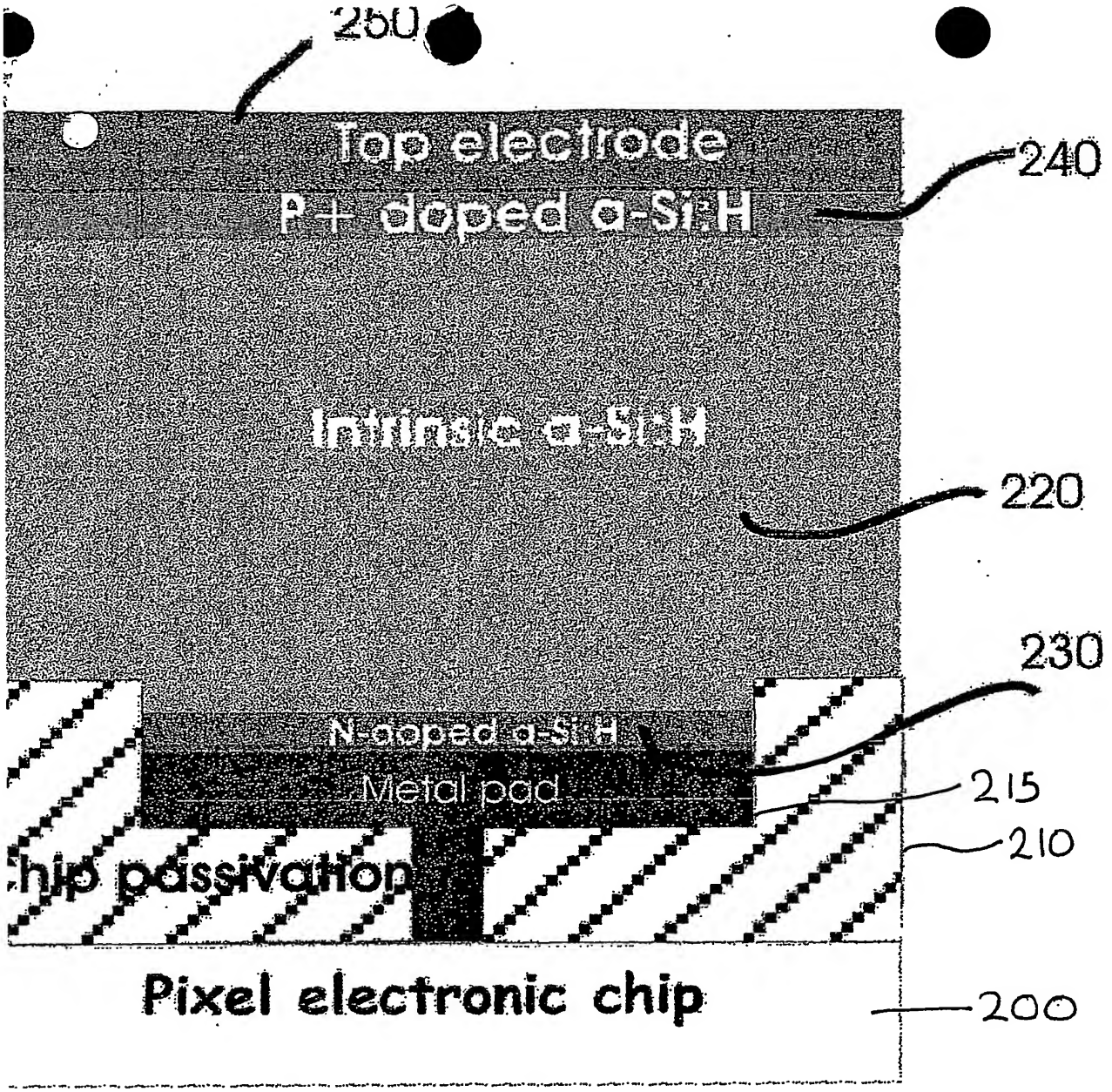

250
Top electrode
P+ doped a-Si:H
240
Intrinsic a-Si:H
220
230
N-doped a-Si:H
Metal pad
215
210
Chip passivation
Pixel electronic chip
200

Figure 15

FIG.16a

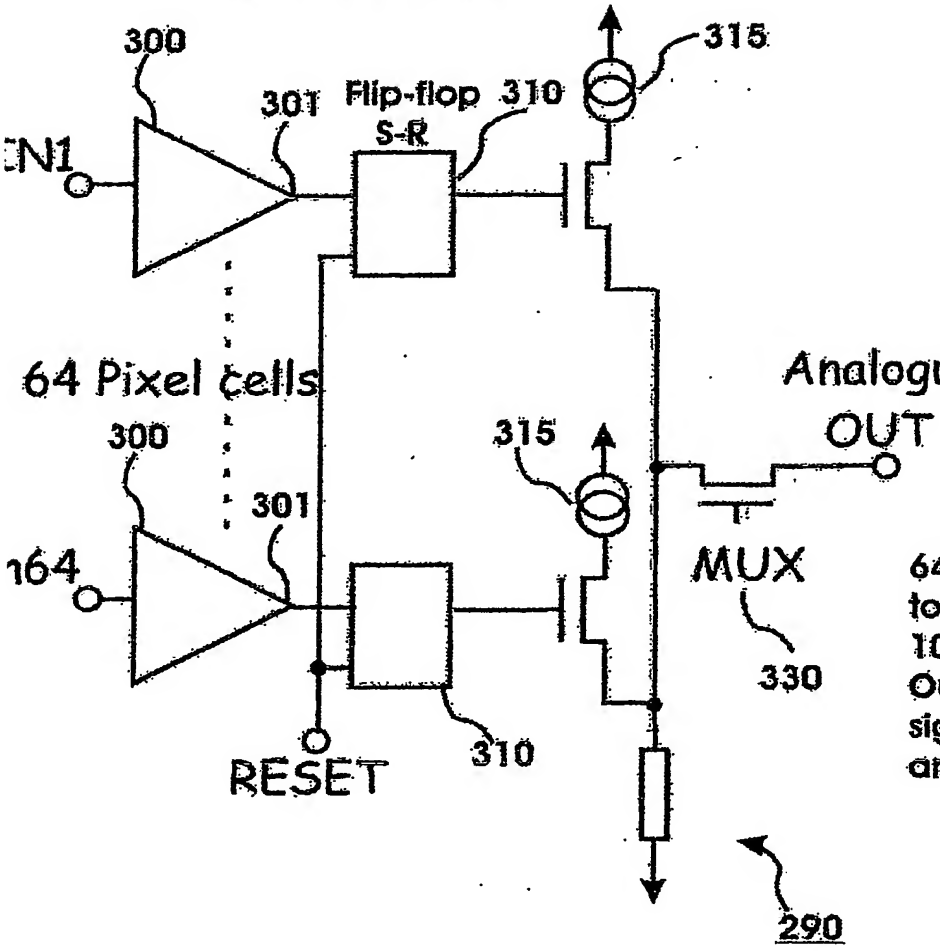
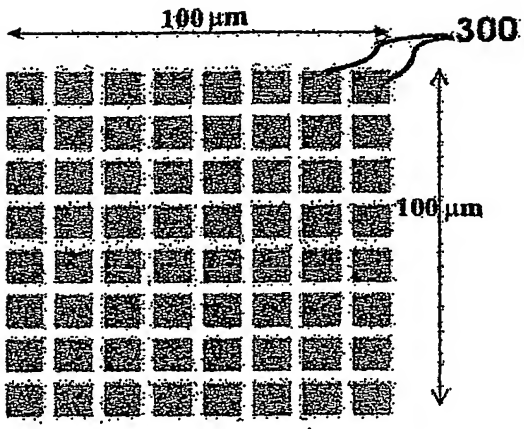


FIG.16b



64 pixels of 12,5microns grouped together forming a macro-pixel of 100 micron x 100 micron
Output is binary weighted analogue signal processed as in standard APS analog readout architecture